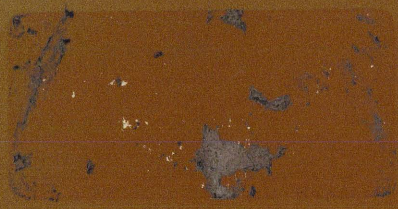
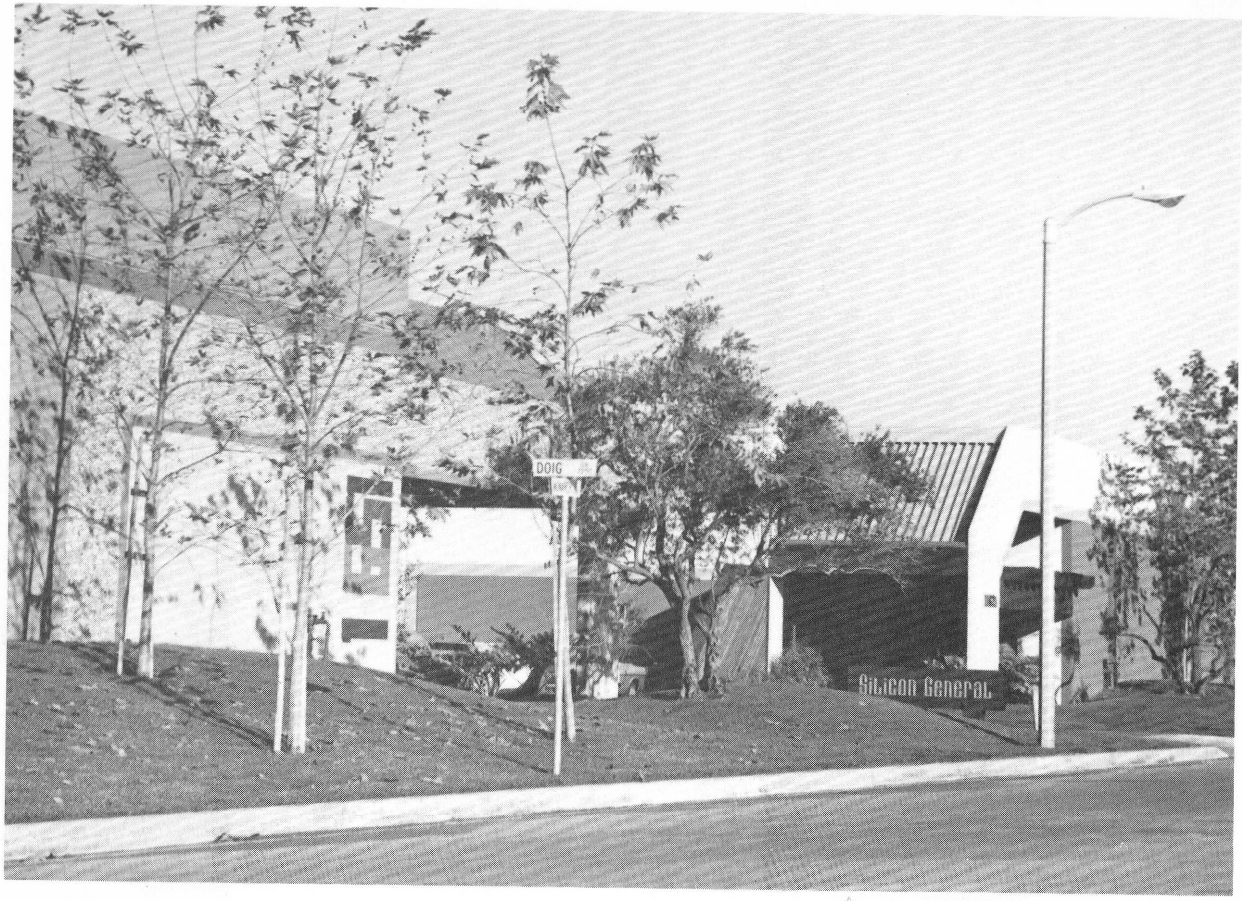


VOLTAGE REGULATORS
OPERATIONAL AMPLIFIERS
INTERFACE CIRCUITS
TRANSISTOR ARRAYS
OTHER CIRCUITS

SILICON GENERAL
Linear Integrated Circuits

product
catalog
1979



INTRODUCTION

Silicon General is committed to innovative excellence in the manufacture of integrated circuits. A unique combination of design and processing skills developed over the past ten years results in the continual generation of leadership solid state products.

All Silicon General devices are processed in the finest facilities available in strict accordance with the requirements of MIL-STD-883 level B and a complete range of screening and testing capabilities to higher levels is available.

This book describes Silicon General's complete line of products and includes information which will allow you to both specify and apply these products. Also included is a section describing our quality and reliability program.

If you need more information on these products or on other applications, please contact the nearest Silicon General representative listed in the back of this product catalog.

PRODUCT SELECTOR GUIDE

REGULATORS

OPERATIONAL AMPLIFIERS

INTERFACE CIRCUITS

TRANSISTOR ARRAYS

OTHER CIRCUITS

APPLICATIONS NOTES

OTHER INFORMATION

*Contact factory for data.

Data subject to change without notice.

ORDERING INFORMATION

Inquiries may be directed to the nearest distributor, representative or the factory. Headquarters' offices are located at 11651 Monarch Street, Garden Grove, California 92641. Telephone: (714) 892-5531, TWX: 910-596-1804. Telex. 69-2411.

MIL-STD-883 Program – Parts tested and processed to 883 Level A, B or C are marked with the appropriate level immediately after the part no., i.e., SG101AT/883A, SG101AT/883B, SG101AT/883C.

Integrated Circuit Marking and Product Code Explanation – Where Silicon General is second-sourcing an existing device, the company will use the number assigned by the company which introduced the circuit, adding only an SG prefix.

Part number may include suffix letter "A" indicating an improved electrical specification (SG101AT). Suffix letter "C" indicates Commercial temperature range (SG741CT).

Federal Supply Code Number – Silicon General's Federal Manufacturer's Supply Code Number is 34333.

WHEN ORDERING STANDARD PRODUCT

Specify:

- Generic part number (Includes designation for both electrical grade and temperature range)
- Package type (see Table A, below)

Example:

SG 1524 J
(1) (2) (3)

(1) = Silicon General manufacture
(2) = Generic part type
(3) = Ceramic dual-in-line package

WHEN ORDERING MIL-STD-883 SCREENED PRODUCT

Specify:

- Generic part number (prime electrical and -55°C to +125°C temperature range is standard)
- Package type (see Table A below)
- Class of 883 screening

Example:

SG 1524 J / 883 B
(1) (2) (3) (4) (5)

(1) = Silicon General manufacture
(2) = Generic part type
(3) = Ceramic dual-in-line package
(4) = Full screening to MIL-STD-883A
(5) = Class B screening level

WHEN ORDERING CHIPS

Refer to appropriate technical data sheet for schematic diagrams, electrical characteristics and other data. Order by SG type numbers. All chips are 100% electrically tested @25°C to minimum specifications on all key parameters. All chip lots are visually inspected per MIL-STD-883, Method 2010, Condition B minimum. Unless otherwise requested, visual characteristics are guaranteed to a 10% LTPD.

All chip lots contain units which will meet both 0°C to +70°C and -55°C to +125°C temperature ranges. Chips can be guaranteed to military temperature range (-55°C to +125°C specifications) upon special request. Chips can also be guaranteed to meet special parameter limits. Consult factory for details.

All chips are available with gold backing. Please specify at time of order if back metalization is required. Electrically tested, inked wafers (scribed and unscribed) are also available (20% LTPD).

Chips are shipped in 100-unit trays. Minimum order: $250.00 for standard device. Contact factory for additional pricing and delivery.

TABLE B

Lead Finish Description	38510 Designator
Hot Solder Dip	A
Acid Tin Plate	B
Gold Plate	C

TABLE A

Package Description	Silicon General Package Designation*	MIL-M-38510 Package Designation	Package Description	Silicon General Package Designation	MIL-M-38510 Package Designation
2 Pin Metal Can TO-3	K	Y	16 Pin 1/4" x 7/8" Plastic Dip	N	–
2 Pin Metal Can TO-66	R	–	8 Pin 1/4" x 3/8" Ceramic Minidip	Y	P
3 Pin Metal Can TO-5 or TO-39	T	X	14 Pin 1/4" x 3/4" Ceramic Dip	J	C
3 Pin 3/8" x 3/8" Plastic TO-220	P	–	16 Pin 1/4" x 7/8" Ceramic Dip	J	E
8 Pin Metal Can TO-99	T	G	14 Pin 1/4" x 3/4" Metal/Glass Dip	D	C
9 Pin Metal Can TO-66	R	–	16 Pin 1/4" x 3/4" Metal/Glass Dip	D	E
10 Pin Metal Can TO-100 & TO-96	T	I	10 Pin 1/4" x 1/4" Metal Flat Pack	F	H
12 Pin Metal Can TO-101	T	M	14 Pin 1/4" x 1/4" Metal Flat Pack	F	A
8 Pin 1/4" x 3/8" Plastic Minidip	M	–	16 Pin 1/4" x 3/8" Metal Flat Pack	F	F
14 Pin 1/4" x 3/4" Plastic Dip	N	–			

*See page 166 for details of package outlines.

CROSS REFERENCE

PACKAGE SUFFIXES

Package	Silicon General	National	Fairchild	Texas Instruments	Motorola	RCA	Raytheon	Signetics
3, 8, 10 Pin Metal Can	T	H	H	L	G	T	T	T
8 Pin Plastic DIL	M	N	T	P	PI	E	N	V
14, 16 Pin Plastic DIL	N	N	P	N	P	E	CH DB	N
14, 16 Pin Ceramic DIL	J	J	D	J	L	F	DC DD	F
3 Pin TO-3 Power	K	K	K	—	K	—	LK	DA
8 Pin Ceramic DIL	Y	—	—	—	U	—	—	I
3 Pin TO-220 Plastic	P	T	U	K	T	—	Y	—
3, 9 Pin TO-66 Power	R	—	J	—	R	—	TK	DF

See page 169 for addition of package information.

RAYTHEON

Raytheon	SG Direct Replacement	Raytheon	SG Direct Replacement	Raytheon	SG Direct Replacement	Raytheon	SG Direct Replacement
RM101D	SG101D	RC105T	SG305T	RC723D	SG723CD	RC1458T	SG1458T
RM101Q	SG101F	RC105AT	SG305AT	RM723T	SG723T	RC1488D	SG1488J
RM101T	SG101T	RC107D	SG307D	RC723T	SG723CT	RC1489D	SG1489J
RM101AD	SG101AD	RC107Q	SG307F	RC723DP	SG723CN	RC1489AJ	SG1489AJ
RM101AQ	SG101AF	RC107DN	SG307M	RM733D	SG733D	RC1556T	SG1456AT
RM101AT	SG101AT	RC107DP	SG307N	RC733D	SG733CD	RC1556T	SG1456T
RM105Q	SG105F	RC107T	SG307T	RM733T	SG733T	RM1556AT	SG1556AT
RM105T	SG105T	RC108D	SG308D	RC733T	SG733CT	RM1556T	SG1556T
RM107D	SG107D	RC108Q	SG308F	RC733DP	SG733CN	RC1558T	SG1558T
RM107Q	SG107F	RC108T	SG308T	RM741D	SG741D	RM4194L	SG4194J
RM107T	SG107T	RC108AD	SG308AD	RC741D	SG741CD	RC4194L	SG4194CJ
RM108D	SG108D	RC108AT	SG308AT	RM741Q	SG741F	RM4194TK	SG4194R
RM108Q	SG108F	RC109H	SG309T	RC741Q	SG741CF	RC4194TK	SG4194CR
RM108T	SG108T	RC109L	SG309K	RM741T	SG741T	RC7520M	SG7520J
RM108AD	SG108AD	RM555T	SG555T	RC741T	SG741CT	RC7520MP	SG7520N
RM108AQ	SG108AF	RC555T	SG555CT	RC741DN	SG741CM	RC7521M	SG7521J
RM108AT	SG108AT	RC555N	SG555CM	RC741DP	SG741CN	RC7521MP	SG7521N
RM109H	SG109T	RM710T	SG710T	RM747D	SG747D	RC7522M	SG7522J
RM109L	SG109K	RM710AT	SG710AT	RM747T	SG747T	RC7522MP	SG7522N
RM101T	SG301T	RC710T	SG710CT	RC747DF	SG747CD	RC7523M	SG7523J
RC101AD	SG301AD	RC710DP	SG710CN	RC747T	SG747CT	RC7523MP	SG7523N
RC101AQ	SG301AF	RM711T	SG711T	RM748T	SG748T	RC7524M	SG7524J
RC101DN	SG301AM	RC711T	SG711CT	RC748T	SG748CT	RC7524MP	SG7524N
RC101DP	SG301AN	RC711DP	SG711CN	RC748DP	SG748N	RC7525M	SG7525J
RC101AT	SG301AT	RM723D	SG723D	RC1458N	SG1458M	RC7525MP	SG7525N
RC105DP	SG305N						

FAIRCHILD

Fairchild	SG Direct Replacement	Fairchild	SG Direct Replacement	Fairchild	SG Direct Replacement
710F	SG710F	747DC	SG747CD	7815HM	SG7815T
710H	SG710T	747AHM	SG747AT	7815HC	SG7815CT
710HC	SG710CT	747ADM	SG747AJ	7815KM	SG7815K
710D	SG710D	747EHC	SG747ET	7815KC	SG7815CK
710DC	SG710CD	747EDC	SG747EJ	7818HM	SG7818T
711F	SG711F	748F	SG748F	7818HC	SG7818CT
711H	SG711T	748H	SG748T	7818KM	SG7818K
711D	SG711D	748HC	SG748CT	7818KC	SG7818CK
711DC	SG711CD	748D	SG748D	7824HM	SG7824T
723H	SG723T	748DC	SG748CD	7824HC	SG7824CT
723HC	SG723CT	776H	SG1250T*	7824KM	SG7824K
723D	SG723D	776HC	SG3250T*	7824KC	SG7824CK
723DC	SG723CD	777H	SG777T	9665D	SG2001J
733F	SG733F	777HC	SG777CT	9666D	SG2002J
733H	SG733T	777CT	SG777CM	9667D	SG2003J
733HC	SG733CT	7805HM	SG7805T	78M05HM	SG7805T*
733D	SG733D	7805HC	SG7805CT	78M06HM	SG7806T*
733DC	SG733CD	7805KM	SG7805K	78M08HM	SG7808T*
741F	SG741F	7805KC	SG7805CK	78M12HM	SG7812T*
741H	SG741T	7806HM	SG7806T	78M15HM	SG7815T*
741HC	SG741CT	7806HC	SG7806CT	78M24HM	SG7824T*
741D	SG741D	7806KM	SG7806K	78M05HC	SG7805CT*
741DC	SG741CD	7806KC	SG7806CK	78M06HC	SG7806CT*
741CT	SG741CM	7808HM	SG7808T	78M08HC	SG7808CT*
741AHM	SG741AT	7808HC	SG7808CT	78M12HC	SG7812CT*
741ADM	SG741AJ	7808KM	SG7808K	78M15HC	SG7815CT*
741EHC	SG741ET	7808KC	SG7808CK	78M24HC	SG7824CT*
741EDC	SG741EJ	7812HM	SG7812T	75450AN	SG75450BN
747H	SG747T	7812HC	SG7812CT	75450AJ	SG75450BJ
747HC	SG747CT	7812KM	SG7812K	75460AJ	SG75460J
747D	SG747D	7812KC	SG7812CK	75460AN	SG75460N

*Similar, not identical

MOTOROLA

Motorola	SG Direct Replacement	Motorola	SG Direct Replacement	Motorola	SG Direct Replacement
MC1436G	SG1436T	MC1711CF	SG711CF	MC7806CG	SG7806CT
MC1436CG	SG1436CT	MC1711CG	SG711CT	MC7806K	SG7806K
MC1455CG	SG555CT	MC1711CL	SG711CD	MC7806CK	SG7806CK
MC1455CP 1	SG555CM	MC1711F	DG711F	MC7808G	SG7808T
MC1456CG	SG1456CT	MC1711G	SG711T	MC7808CG	SG7808CT
MC1456G	SG1456T	MC1711L	SG711D	MC7808K	SG7808K
MC1458P 1	SG1458M	MC1723CG	SG723CT	MC7808CK	SG7808CK
MC1458G	SG1458T	MC1723G	SG723T	MC7812G	SG7812T
MC1468G	SG1468T	MC1723CL	SG723CD	MC7812CG	SG7812CT
MC1468L	SG1468J	MC1723L	SG723D	MC7812K	SG7812K
MC1468P	SG1468N	MC1741CF	SG741CF	MC7812CK	SG7812CK
MC1488L	SG1488J	MC1741CG	SG741CT	MC7815G	SG7815T
MC1489L	SG1489J	MC1741CL	SG741CD	MC7815CG	SG7815CT
MC1489AL	SG1489AJ	MC1741CP-1	SG741CM	MC7815K	SG7815K
MC1495L	SG1495D	MC1741CP-2	SG741CN	MC7815CK	SG7815CK
MC1496G	SG1496T	MC1741F	SG741F	MC7818G	SG7818T
MC1536G	SG1536T	MC1741G	SG741T	MC7818CG	SG7818CT
MC1555G	SG555T	MC1741L	SG741D	MC7818K	SG7818K
MC1556G	SG1556T	MC1741SG	SG741ST	MC7818CK	SG7818CK
MC1558G	SG1558T	MC1741SCG	SG741SCT	MC7824G	SG7824T
MC1568G	SG1568T	MC1741SCP-1	DG741SCM	MC7824CG	SG7824CT
MC1568L	SG1568J	MC1748G	SG748T	MC7824K	SG7824K
MC1595L	SG1595D	MC1748CG	SG748CT	MC7824CK	SG7824CK
MC1596G	SG1596T	MC3302P-I	SG3302N	MC7905CK	SG320K-05
MC1710CF	SG710CF	MC3302L	SG3302L	MC7912CK	SG320K-12
MC1710CG	SG710CT	MC7805G	SG7805T	MC7915CK	SG320K-15
MC1710CL	SG710CD	MC7805CG	SG7805CT	MC7952CK	SG320K-5.2
MC1710F	SG710F	MC7805K	SG7805K	MC75450P	SG75450BN
MC1710G	SG710T	MC7805CK	SG7805CK	MC75450L	SG75450BJ
MC1710L	SG710D	MC7806G	SG7806T		

iUIDE

NATIONAL

National	SG Direct Replacement	National	SG Direct Replacement	National	SG Direct Replacement	National	SG Direct Replacement
LM100H	SG100T	LM140K-18	SG140K-18	LM309H	SG309T	LM723CH	SG723CT
LM101D	SG101D	LM140H-24	SG140T-24	LM309K	SG309K	LM723CN	SG723CN
LM101F	SG101F	LM140K-24	SG140K-24	LM310H	SG310T	LM741F	SG741F
LM101H	SG101T	LM200H	SG200T	LM311H	SG311T	LM741H	SG741T
LM101AD	SG101AD	LM201H	SG201T	LM312H	SG3118AT	LM741CH	SG741CT
LM101AF	SG101AF	LM201AH	SG201AT	LM317T	SG317T	LM741CN	SG741CM
LM101AH	SG101AT	LM202H	SG202T	LM317K	SG317K	LM741AD	SG741AJ
LM102H	SG102T	LM204H	SG204T	LM320H-05	SG320T-05	LM741AH	SG741AT
LM104H	SG104T	LM205H	SG205T	LM320K-05	SG320K-05	LM747D	SG747D
LM105F	SG105F	LM207H	SG207T	LM320H-5.2	SG320T-5.2	LM747CD	SG747CD
LM105H	SG105T	LM208H	SG208T	LM320K-5.2	SG320K-5.2	LM747F	SG747F
LM107D	SG107D	LM209H	SG209T	LM320H-12	SG320T-12	LM747H	SG747T
LM107F	SG107F	LM210H	SG210T	LM320K-12	SG320K-12	LM747CH	SG747CT
LM107H	SG107T	LM211H	SG211T	LM320H-15	SG320T-15	LM747CN	SG747CN
LM108D	SG108D	LM212H	SG2118AT	LM320K-15	SG320K-15	LM747AD	SG747AJ
LM108F	SG108F	LM217T	SG217T	LM323K	SG323K	LM747AH	SG747AT
LM108H	SG108T	LM217K	SG217K	LM324D	DG324J	LM748H	SG748T
LM108AD	SG108AD	LM220H-05	SG220T-05	LM324N	SG324N	LM748CH	SG748CT
LM108AF	SG108AF	LM220K-05	SG220K-05	LM339D	SG339J	LM748CN	SG748CM
LM108AH	SG108AT	LM220H-5.2	SG220T-5.2	LM339AD	SG339AJ	LM1458N	SG1458M
LM109H	SG109T	LM220K-5.2	SG220K-5.2	LM339N	SG339N	LM1458H	SG1458T
LM109K	SG109K	LM220H-12	SG220T-12	LM339AN	SG339AN	LM1496N	SG1496N
LM110H	SG110T	LM220K-12	SG220K-12	LM340H-05	SG340T-05	LM1496H	SG1496T
LM111H	SG111T	LM220H-15	SG220T-15	LM340K-05	SG340K-05	LM1558H	SG1558T
LM112H	SG1118AT	LM220K-15	SG220K-15	LM340H-06	SG340T-06	LM1596H	SG1596T
LM117T	SG117T	LM223K	SG223K	LM340K-06	SG340K-06	LM3302D	SG3302J
LM117K	SG117K	LM224D	SG224J	LM340H-08	SG340T-08	LM3302N	SG3302N
LM120H-05	SG120T-05	LM239D	SG239J	LM340K-08	SG340K-08	LM4250H	SG4250T
LM120K-05	SG120K-05	LM239AD	SG239AJ	LM340H-12	SG340T-12	LM4250CH	SG4250CT
LM120H-5.2	SG120T-5.2	LM239N	SG239N	LM340K-12	SG340K-12	LM4250CN	SG4250CM
LM120K-5.2	SG120K-5.2	LM239AN	SG239AN	LM340H-15	LM340T-15	LM7520D	SG7520J
LM120H-12	SG120T-12	LM300H	SG300T	LM340K-15	LM340K-15	LM7520N	SG7520N
LM120K-12	SG120K-12	LM301AH	SG301AT	LM340H-18	LM340T-18	LM7521D	SG7521J
LM120H-15	SG120T-15	LM301AD	SG301AD	LM340K-18	LM340K-18	LM7521N	SG7521N
LM120K-15	SG120K-15	LM301AF	SG301AF	LM340H-24	LM340T-24	LM7522D	SG7522J
LM123K	SG123K	LM301AN	SG301AM	LM340K-24	LM340K-24	LM7522N	SG7522N
LM124D	SG124J	LM302H	SG302T	LM367N	SG305M	LM7523D	SG7523J
LM139D	SG139J	LM304H	SG304T	LM555H	SG555T	LM7523N	SG7523N
LM139AD	SG139AJ	LM305H	SG305T	LM555C	SG555CT	LM7524D	SG7524J
LM140H-05	SG140T-05	LM305AH	SG305AT	LM555N	SG555CM	LM7524N	SG7524N
LM140K-05	SG140K-05	LM307D	SG307D	LM710H	SG710T	LM7525D	SG7525J
LM140H-06	SG140T-06	LM307F	SG307F	LM710AH	SG710AT	LM7525N	SG7525N
LM140K-06	SG140K-06	LM307H	SG307T	LM710CH	SG710CT	LM7528D	SG7528J
LM140H-08	SG140T-08	LM307N	SG308M	LM710CN	SG710CN	LM7528N	SG7528N
LM140K-08	SG140K-08	LM308D	SG308D	LM711H	SG711T	LM7529D	SG7529J
LM140H-12	SG140T-12	LM308F	SG308F	LM711CH	SG711CT	LM7529N	SG7529N
LM140K-12	SG140K-12	LM308H	SG308T	LM711CN	SG711CN	LM75450N	SG75450BN
LM140H-15	SG140T-15	LM308AD	SG308AD	LM723D	SG723D		
LM140K-15	SG140K-15	LM308AF	SG308AF	LM723CD	SG723CD		
LM140H-18	SG140T-18	LM308AH	SG308AT	LM723H	SG723T		

SIGNETICS

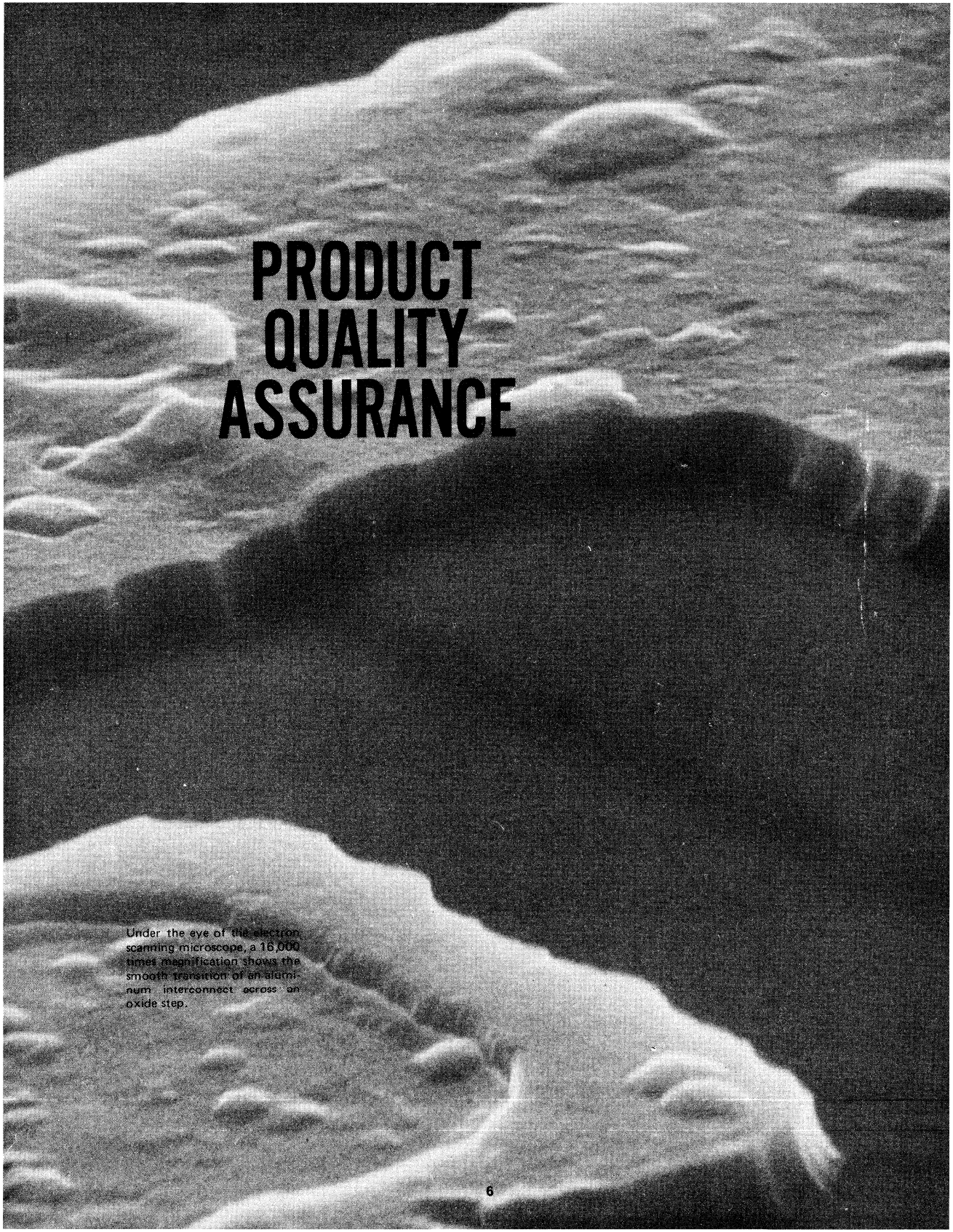
Signetics	SG Direct Replacement		
LM1001AF	SG101AD	μA711CA	SG711CN
LM101AK	SG101AT	μA711CK	SG711CT
LM101F	SG101D	μA723L	SG723T
LM101Q	SG101F	μA723CL	SG723CT
LM101K	SG101T	μA723CA	SG723CN
LM107K	SG107T	μA733K	SG733T
LM109DB	SG109T	μA733I	SG733J
LM109DA	SG109K	μA733CA	SG733CN
LM201AF	SG201AD	μA733CK	SG733CT
LM201AK	SG201AT	μA733CI	SG733CJ
LM201DF	SG201D	μA741T	SG741T
LM201K	SG201T	μA741CA	SG741CN
LM201AN-14	SG201AN	μA741CT	SG741CT
LM201Y	SG201M	μA741CV	SG741CM
LM201Q	SG201F	μA747T	SG747T
LM207K	SG207T	μA747CA	SG747CN
LM207Y	SG207M	μA747CK	SG747CT
LM209DB	SG209T	μA748T	SG748T
LM209KDA	SG209K	μA748CA	SG748CN
LM301AF	SG301AD	μA748CT	SG748CT
LM301AH	SG301AT	μA748CV	SG748CM
LM301AN-14	SG301AN	S5556K	SG1556T
LM301AN	SG301AM	N5556K	SG1456T
LM307K	SG307T	N5556V	SG1456M
LM307A	SG307M	S558K	SG1558T
LM309DB	SG309T	N5558K	SG1458T
LM309K	SG309K	N5558V	SG1458M
SE555K	SG555CT	S5596K	SG1596T
NE555F	SG555CT	N5596A	SG1496N
NE555Y	SG555CM	N5596K	SG1496T
SE556K	SG556T	SN7520A	SG7520N
NE556K	SG556CT	SN7521A	SG7521N
μA710Q	SG710F	SN7522A	SG7522N
μA710K	SG710T	SN7523A	SG7523N
μA710CA	SG710CN	SN7524A	SG7524N
μA710CK	SG710CT	SN7525A	SG7525N
μA711Q	SG711F	SN75450A	SG75450BN
μA711H	SG711T		

RCA

RCA	SG Direct Replacement		
CA3001	SG3001	CA3083E	SG3083N
CA3018T	SG3018T	CA3083F	SG3083J
CA3018AT	SG3018AT	CA3086E	SG3086N
CA3026T	SG3822T	CA3086F	SG3086J
CA3045F	SG3821J	CA3146E	SG3146N
CA3046E	SG3821N	CA3183E	SG3183N
CA3054E	SG3822N	CA3183AE	SG3183AN
CA3055T	SG300T	CA3741T	SG3741T
CA3058F	SG3058J	CA3741CT	SG741CT
CA3059F/E	SG3059J/N	CA3747CT	SG747CT
CA3079E	SG3079N	CA3747E	SG747N
CA3081E	SG3081N	CA3747T	SG747T
CA3081F	SG3081J	CA3748CT	SG748CT
CA3082E	SG3082N	CA3748T	SG748T
CA3082F	SG3082J		

TEXAS INSTRUMENTS

Texas Instruments	SG Direct Replacement	Texas Instruments	SG Direct Replacement	Texas Instruments	SG Direct Replacement	Texas Instruments	SG Direct Replacement	Texas Instruments	SG Direct Replacement	Texas Instruments	SG Direct Replacement
ULN2001J	SG2001J	SN52108L	SG108T	SN55450BJ	SG55450BJ	SN72308J	SG308D	SN7520J	SG7520J	SN75138J	SG75138J
ULN2002J	SG2002J	SN52108AF	SG108AF	SN55451J	SG55451J	SN72308L	SG308T	SN7520N	SG7520N	SN75138N	SG75138N
ULN2003J	SG2003J	SN52108AJ	SG108AD	SN55452J	SG55452J	SN72308AZ	SG308AF	SN7521J	SG7521J	SG75154J	SG75154J
SN5520J	SG5520J	SN52108AL	SG108AT	SN55453J	SG55453J	SN72308J	SG308D	SN7521N	SG7521N	SG75325J	SG75325J
SN5521J	SG5521J	SN52555L	SG555T	SN55454J	SG55454J	SN72308L	SG308T	SN7522J	SG7522J	SN75325N	SG75325N
SN5522J	SG5522J	SN52710J	SG710D	SN55460J	SG55460J	SN72555L	SG555CT	SN7522N	SG7522N	SN75450BN	SG75450BN
SN5523J	SG5523J	SN52710L	SG710T	SN55461J	SG55461J	SN72555P	SG555CM	SN7523J	SG7523J	SN75450BJ	SG75450BJ
SN5524J	SG5524J	SN52710S	SG710F	SN55462J	SG55462J	SN72710J	SG710CD	SG7523N	SG7523N	SN75451J	SG75451J
SN5525J	SG5525J	SN52711J	SG711D	SN55463J	SG55463J	SN72710L	SG710CT	SN7524J	SG7524J	SN75452J	SG75452J
SN5526J	SG5526J	SN52711L	SG711T	SN55464J	SG55464J	SN72711J	SG711CD	SN7524N	SG7524N	SN75453J	SG75453J
SN5527J	SG5527J	SN52711Z	SG711F	SN55471J	SG55471J	SN72711L	SG711CT	SN7525J	SG7525J	SN75454J	SG75454J
SN5528J	SG5528J	SN52733L	SG733T	SN55472J	SG55472J	SN72733L	SG733CT	SN7525N	SG7525N	SN75460N	SG75460N
SN5529J	SG5529J	SN52733N	SG733N	SN55473J	SG55473J	SN72733N	SG733CD	SN7528J	SG7528J	SN75460J	SG75460J
SN5534J	SG5534J	SN52741F	SG741F	SN55474J	SG55474J	SN72741Z	SG741CF	SN7528N	SG7528N	SN75461J	SG75461J
SN5535J	SG5535J	SN52741J	SG741D	SN72301J	SG101D	SN72741J	SG741CD	SN7529J	SG7529J	SN75462J	SG75462J
SN5536J	SG5536J	SN52741L	SG741T	SN72301L	SG201T	SN72741L	SG741CT	SN7529N	SG7529N	SN75463J	SG75463J
SN5537J	SG5537J	SN52747J	SG747D	SN72301Z	SG201F	SN72741P	SG741CM	SN7534J	SG7534J	SN75464J	SG75464J
SN5538J	SG5538J	SN52747L	SG747T	SN72301AJ	SG301AD	SN72741N	SG741CN	SN7534N	SG7534N	SN75471J	SG75471J
SN5539J	SG5539J	SN52748F	SG748F	SN72301AL	SG301AT	SN72747J	SG747CD	SN7535J	SG7535J	SN75472J	SG75472J
SN52107J	SG107D	SN52748J	SG748D	SN72301AZ	SG301AF	SN72747L	SG747CT	SN7535N	SG7535N	SN75473J	SG75473J
SN52107L	SG107T	SN52748L	SG748T	SN72307J	SG307D	SN72747M	SG747CN	SN7538J	SG7538J	SN75474J	SG75474J
SN52107Z	SG107F	SN55138J	SG55138J	SN72307L	SG307T	SN72748F	SG748CF	SN7538N	SG7538N	SG1524	SG1524
SN52108F	SG108F	SN55154J	SG55154J	SN72307Z	SG307F	SN72748J	SG748CD	SN7539J	SG7539J	SG2524	SG2524
SN52108J	SG108D	SN55325J	SG55325J	SN72308Z	SG308F	SN72748L	SG748CT	SN7539N	SG7539N	SG3524	SG3524



PRODUCT QUALITY ASSURANCE

Under the eye of the electron scanning microscope, a 16,000 times magnification shows the smooth transition of an aluminum interconnect across an oxide step.

SG104/204/304

This circuit is a negative voltage regulator designed for both linear and switching applications. It is a complement of the SG100/200/300, SG105/205/305 and SG723/723C intended for systems requiring regulated negative voltages having a common ground with the unregulated supply. With an input voltage rating of up to 50V, this device will deliver load currents to 25mA. Adding external transistors will increase the current capability to greater than 10 amps and further improve regulation.

- **Output voltage adjustable from 15mV to 40V**
- **1mV regulation no load to full load**
- **0.01%/V line regulation**
- **1% maximum temperature variation**

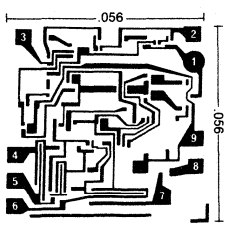
PARAMETERS*	104	204	304	UNITS
Operating Temperature Range	−55 to +125	−25 to +85	0 to +70	°C
Package Types	T			
Input Voltage Range	−50 to −8		−40 to −8	V
Output Voltage Range	−40 to −0.015		−30 to −0.035	V
Input/Output Differential I_o = 20 mA[1]	2.0 to 50		2.0 to 40	V
Load Regulation[2] $0 \leq I_o \leq 20$ mA, $R_{sc} = 15\Omega$	5mV			–
Line Regulation[3] $V_{out} \leq -5V$, $\Delta V_{in} = 0.1\ V_{in}$	0.1			%
Ripple Feed thru $C_{19} = 10\mu f$, f = 120Hz, $-7V \leq V_{in} \leq -15V$	1.0		1.0	mV/V
Output Voltage Scale Factor $R_{23} = 2.4k\Omega$	1.8 to 2.2		1.8 to 2.2	V/kΩ
Temperature Stability $V_o \leq -1V$	1.0		1.0	%
Output Noise Voltage $C_{19} = 0\mu F$ BW = 10Hz to 10KHz $V_o \leq -5V$	0.007 (typ)		0.007 (typ)	%
Standby Current Drain $V_o = 0$, $I_L = 5$ mA	2.5		2.5	mA
Long Term Stability $V_o \leq -1V$	1.0		1.0	%

*Parameters apply at junction temperatures equal to or less than operating temperature range unless otherwise specified. The line and load regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

[1] With I_o = 5 mA, min differential is 0.5V. With external transistors differential is increased, in the worst case, by approx. 1V.

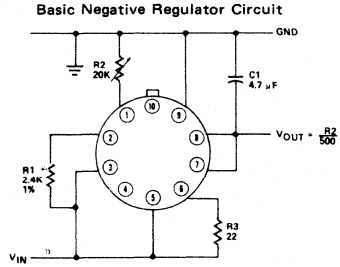
[2] Output current and load regulation can be improved with external transistors. Improvement factor will be approx. equal to the composite current gain of added transistors.

[3] With zero output, the dc line regulation is determined from the ripple rejection. Hence, with output voltages between 0 volts and −5 volts, a dc output variation, determined from the ripple rejection, must be added to find the worst-case line regulation.

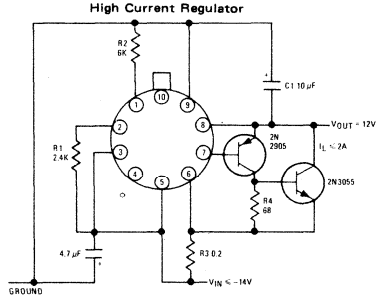


SG104/204/304 Chip (See T-package diagram for pad functions)

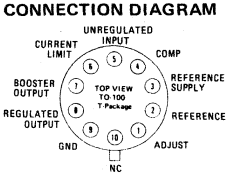
Basic Negative Regulator Circuit



High Current Regulator



CONNECTION DIAGRAM



SG109/209/309

The SG109 series is a completely self-contained 5V regulator. Designed to provide local regulation at currents up to 1 amp for digital logic cards, this device is available in two commonly used transistor packages – the solid header TO–5 and the TO–3 power package.

A major feature of the SG109's design is its built-in protective features which make it essentially blowout proof. These consist of both current limiting to control the peak currents and thermal shutdown to protect against excessive power dissipation. With the only added component being the possible need for an input bypass capacitor, this regulator becomes extremely easy to apply.

- **Fully compatible with TTL and DTL**
- **Output current in excess of 1 amp**
- **Internal thermal overload protection**
- **No additional external components**

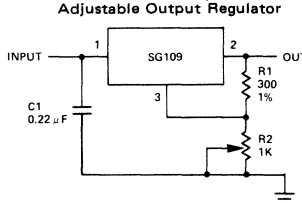
PARAMETERS[1]	109	209	309	UNITS
Operating Temperature Range	–55 to +150	–25 to +150	0 to +125	°C
Package Types	T, K		T, K	–
Output Voltage	4.9 to 5.1		4.8 to 5.2	V
Line Regulation 7V ≤ V_{in} ≤ 25V	50			mV
Load Regulation 5mA ≤ I_{out} ≤ 0.5A (1.5A for TO-3)	TO-5: 50; TO-3: 100			mV
Total Output Voltage Tolerance[2]	4.75 to 5.25			V
Quiescent Current V_{in} ≤ 25V	10			mA
Ripple Rejection 10 Hz ≤ f ≤ 10kHz	75 (typ)			dB
Output Noise Voltage 10Hz ≤ f ≤ 100kHz	40 (typ)			μVrms
Output Impedance 10Hz ≤ f ≤ 10kHz	0.1 (typ)			Ω
Long Term Stability	10			mV

[1] Unless otherwise specified, T_j = 25°C, V_{in} = 10 Volts, and I_{out} = 0.1A.

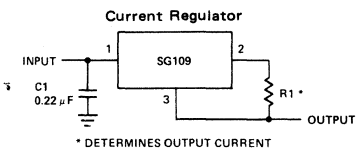
[2] 7V ≤ V_{in} ≤ 25V, 5mA ≤ I_{out} ≤ 1.0A (0.2A for TO-5), P ≤ 20W (2W for TO-5), ΔT_j max.

$T_j$max = –55°C to +150°C for the SG109
= –25°C to +150°C for the SG209
= 0°C to +125°C for the SG309

Adjustable Output Regulator

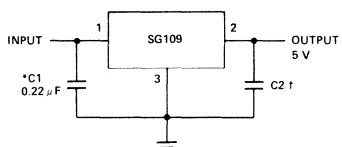


Current Regulator



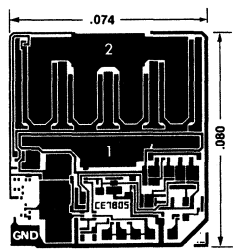
* DETERMINES OUTPUT CURRENT

Fixed 5V Regulator



* REQUIRED IF REGULATOR IS AN APPRECIABLE DISTANCE FROM POWER SUPPLY FILTER.

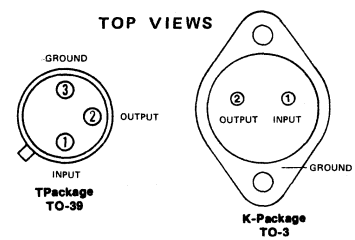
† ALTHOUGH NO OUTPUT CAPACITOR IS NEEDED FOR STABILITY, IT DOES IMPROVE TRANSIENT RESPONSE.



SG109/209/309 Chip

CONNECTION DIAGRAMS

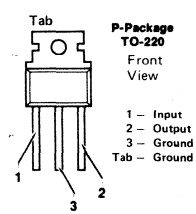
TOP VIEWS



TPackage TO-39

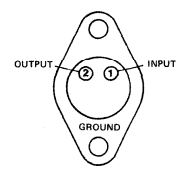
K-Package TO-3

(CASE IS INTERNALLY CONNECTED TO GROUND)



P-Package TO-220
Front View

1 – Input
2 – Output
3 – Ground
Tab – Ground



R-Package TO-66

SG117 / SG217 / SG317

Description

This monolithic integrated circuit is an adjustable 3-terminal positive voltage regulator designed to supply more than 1.5 amps of load current with an output voltage adjustable over a 1.2 to 37 volt range. Although ease of setting the output voltage to any desired value with only two external resistors is a major feature of this circuit, exceptional line and load regulation are also offered. In addition, full overload protection consisting of current limiting, thermal shutdown and safe-area control are included in this device which is packaged in proven-reliability steel TO-3, TO-66 and solid-based TO-39 packages. The SG117 is rated for operation from −55°C to +150°C, the SG217 from −25°C to +150°C and the SG317 from 0°C to +125°C.

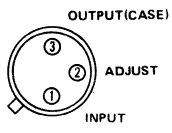
Features

- **Output adjustable between 1.2 and 37 volts**
- **Output current in excess of 1.5 amps**
- **Floating operation for high voltages**
- **0.1% line and load regulation**
- **Full overload protection**
- **High-reliability, hermetically-sealed package**
- **SG317 available in TO-220**

Absolute Maximum Ratings

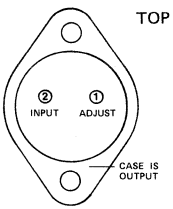
Power Dissipation	Internally Limited
Input-Output Voltage Differential	40V
Storage Temperature	-65°C to +150°C
Operating Junction Temperature Range	
SG117	-55°C to +150°C
SG217	-25°C to +150°C
SG317	0°C to +125°C

CONNECTION DIAGRAMS

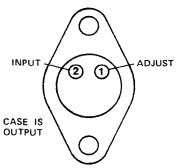


T-Package
TO-39

TOP VIEWS



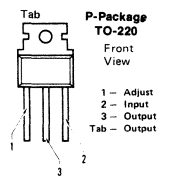
K-Package
TO-3

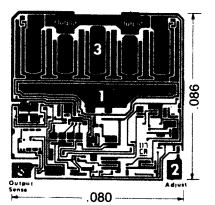


R-Package
TO-66

Electrical Characteristics (See Note)

PARAMETER	CONDITIONS	SG117/217 MIN	SG117/217 TYP	SG117/217 MAX	SG317 MIN	SG317 TYP	SG317 MAX	UNITS
Line Regulation	T_A = 25°C, 3V ≤ (V_{IN} − V_O) ≤ 40V		0.01	0.02		0.01	0.04	%/V
Load Regulation	T_A = 25°C, V_O ≤ 5V		5	15		5	25	mV
	10 mA ≤ I_O ≤ I_{MAX} V_O ≥ 5V		0.1	0.3		0.1	0.5	%
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	2.5V ≤ (V_{IN} − V_O) ≤ 40V, 10 mA ≤ I_O ≤ I_{MAX}		0.2	5		0.2	5	μA
Reference Voltage	3V ≤ (V_{IN} − V_O) ≤ 40V, 10 mA ≤ I_O ≤ I_{MAX}, P ≤ P_{MAX}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	3V ≤ (V_{IN} − V_O) ≤ 40V		0.02	0.05		0.02	0.07	%/V
Load Regulation	T_A = 25°C, C_{ADJ} = 0		20	50		20	70	mV
	f = 120 Hz C_{ADJ} = 10 mfd		0.3	1.0		0.3	1.5	%
Temperature Stability	T_{MIN} ≤ T_j ≤ T_{MAX}		1.0			1.0		%
Minimum Load Current	(V_{IN} − V_O) = 40V		3.5	5.0		3.5	10	mA
Current Limit	(V_{IN} − V_O) ≤ 15V	1.5	2.2		1.5	2.2		A
	(V_{IN} − V_O) = 40V		0.4			0.4		A
Output Noise, RMS	T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz		0.003			0.003		%
Ripple Rejection	T_A = 25°C, C_{ADJ} = 0		65			65		db
	f = 120 Hz C_{ADJ} = 10 mfd	66	80		66	80		db
Long Term Stability	T_A = 125°C		0.3	1		0.3	1	%/khr
Thermal Resistance, Junction to Case	K Package		2.3	3		2.3	3	°C/W
	R Package		5	6		5	6	°C/W
	P Package		3	5		3	5	°C/W
	T Package		12	15		12	15	°C/W





NOTE: Unless otherwise noted, the above specifications apply over the following conditions

SG117: -55°C ≤ T_j ≤ 150°C

SG217: -25°C ≤ T_j ≤ 150°C

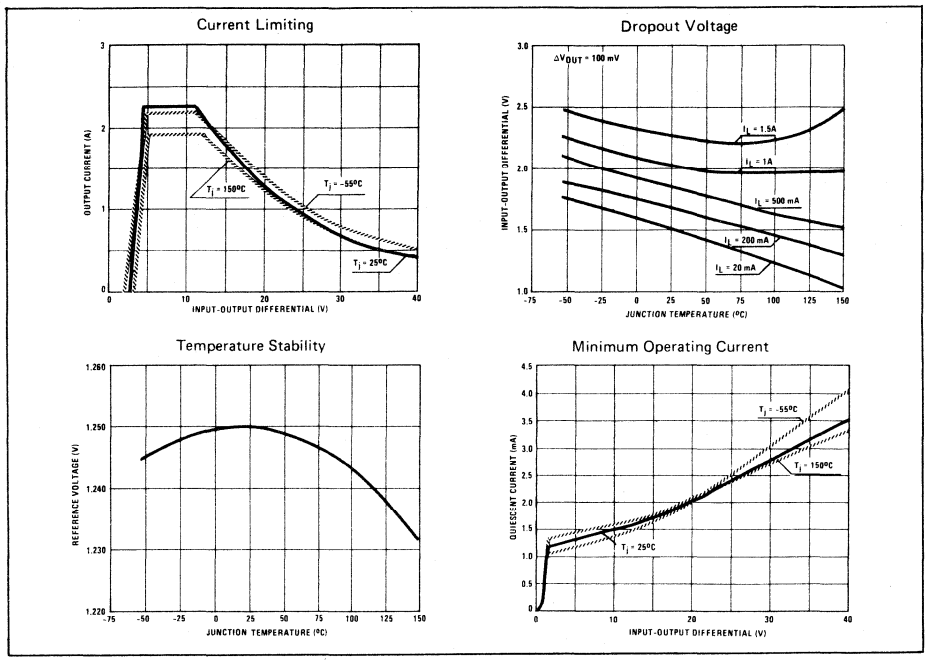
SG317: 0°C ≤ T_j ≤ 125°C

K, R, P-Package: (V_{IN} − V_O) = 5V, I_O = 0.5A, I_{MAX} = 1.5A

T-Package: (V_{IN} − V_O) = 5V, I_O = 0.1A, I_{MAX} = 0.5A

All regulation specifications are measured at constant junction temperatures using low duty-cycle pulse testing.

Typical Performance Characteristics



APPLICATION DATA

The SG117 adjustable 3-terminal regulator is actually designed to provide a fixed 1.25 volt reference voltage between the output and adjustment terminals. This voltage is converted to a programming current by the action of R1 as shown in Figure 1 and this constant current then flows through R2 to ground. The output voltage of the regulator is then:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

Since I_{ADJ} is controlled to less than 100 μA, the error associated with this term is negligible. It should be noted that the method of keeping I_{ADJ} small is to return all the regulator quiescent current to the output terminal. This imposes the requirement for a minimum load current. If the load is less than this minimum, the output will rise.

Since the SG117 is a floating regulator, it is only the input-output voltage differential which is important to regulator performance and operation at high voltages with respect to ground are possible.

Good load regulation can be achieved with the SG117 even without remote sensing, since the case is the output terminal of the regulator which can be a very low impedance point. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible; perhaps even with a separate connection to the case. The ground end of R2 can be used as a remote sense lead and should be connected as close to the load as possible.

No external capacitors are required with the SG117, but in some applications, performance may be improved with added capacitance as follows:

1. An input capacitor at 0.1 mfd will protect against problems when high line impedance is present. The device can be more sensitive to input impedance when output or adjustment capacitors are used.
2. Bypassing the adjustment terminal to ground with a 10 mfd capacitor will improve the ripple rejection by about 15 dB.
3. A 1 mfd tantalum capacitor on the output will improve transient response and keep the regulator from ringing due to light capacitive loading.

In addition to external capacitors, it is sometimes good practice to add protection diodes as shown in Figure 2 if there is a chance that a capacitor may discharge through the regulator IC.

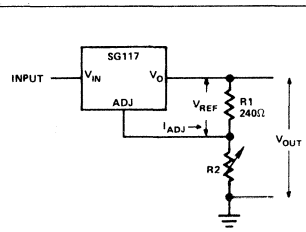


FIGURE 1. Basic Adjustable Regulator Circuit

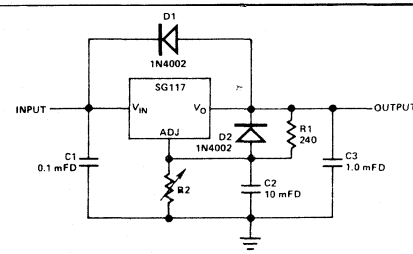


FIGURE 2. Diode D1 protects against C3 with an input short. Diode D2 protects against C2 with an output short.

SG123 / SG223 / SG323

Description

The SG123 is a three terminal, three amp, five volt regulator similar to the LM123 but with a special low voltage zener instead of the band gap reference. The SG123 has superior load regulation, lower input-output differential minimums, lower quiescent current, and better temperature coefficient. The circuit is specified identically to the LM123 and is pin for pin compatible with that device. The SG123 uses special processing techniques to achieve reliable operation at high temperatures and high current levels for extended periods of time.

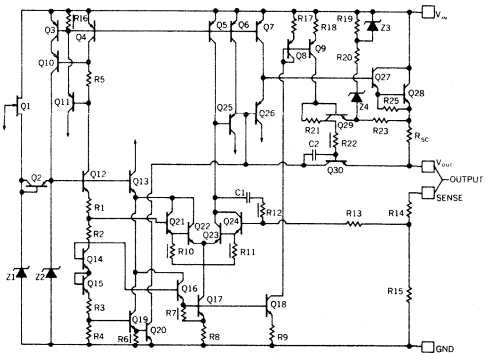
The SG123 has been designed for ease of operation as well as performance. It is completely internally phase compensated, and requires no external capacitors unless used with long lead lengths or high speed transients. The device is protected by thermal shutdown, standard current limiting, and an instantaneous power limiting circuit sensitive to high input voltages. In addition, the power transistor is an upgrade of previous three terminal designs and is unusually rugged.

Operation is guaranteed over the junction temperature range of $-55°C$ to $+150°C$. The SG223 is a similar device guaranteed to operate from $-25°C$ to $+150°C$. The SG323 is guaranteed over the junction temperature range of $0°C$ to $+125°C$.

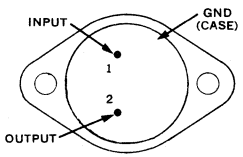
Features

- **3A Output Currents**
- **Full Internal Protection**
- **7.0 V Minimum Input Voltage, Typical**
- **Zener Reference for Top Performance**

SCHEMATIC

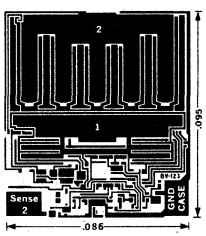


CONNECTION DIAGRAM



TOP VIEW
K-Package
TO-3

CHIP LAYOUT



Absolute Maximum Ratings

Input Voltage	20V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
SG123	$-55°C$ to $+150°C$
SG223	$-25°C$ to $+150°C$
SG323	$0°C$ to $+125°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	SG123/SG223			SG323			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	$T = 25°C$ $V = 7.5V, I = 0$	4.7	5	5.3	4.8	5	5.2	V
Output Voltage	$7.5V \leq V \leq 15V$ $0 \leq I \leq 3A, P \leq 30W$	4.6		5.4	4.75		5.25	V
Line Regulation (Note 2)	$T = 25°C$ $7.5V \leq V \leq 15V$		5	25		5	25	mV
Load Regulation (Note 2)	$T = 25°C, V = 7.5V$ $0 \leq I \leq 3A$		25	100		25	100	mV
Quiescent Current	$7.5V \leq V \leq 15V,$ $0 \leq I \leq 3A$		12	20		12	20	mA
Short Circuit Current Limit	$T = 25°C$ $V = 15V$ $V = 7.5V$		3 4	4.5 5		3 4	4.5 5	A A
Long Term Stability				35			35	mV
Thermal Resistance Junction to Case (Note 3)			2			2		°C/W

Note 1: Unless otherwise noted, specifications apply for $-55°C < T < +150°C$ for the SG123, $-25°C \leq T \leq +150°C$ for the SG223, and $0° \leq T \leq +125°C$ for the SG323. Specifications apply for $P \leq 30W$.

Note 2: Load and line regulation are specified with high speed tests in order to separate their effects from temperature coefficient. Pulse testing is required with a pulse width < 1 ms and a duty cycle $\leq 5\%$.

Note 3: The junction to ambient thermal resistance of the TO-3 package is about 35°C/W.

SG153/SG253/SG353

ADVANCED DATA
SG153/SG253/SG353
Performance data described herein represent design goals.
Final design specifications are subject to change.

DESCRIPTION

The SG153 family of fixed-voltage, three-terminal regulators are designed to supply load currents in excess of three amps over a wide range of operating conditions. Requiring nothing more than a small output capacitor, these regulators feature output voltages internally trimmed to greater than ±2% accuracy. In addition to excellent line regulation, a voltage-boost circuit provides positive load regulation (increasing output voltage with increasing load current) to help correct for line losses.

All protective features of thermal shutdown, current limiting, and safe-area control have been designed into these units with added reliability offered by a hard-solder eutectic die attach and an hermetically sealed TO-3 power package.

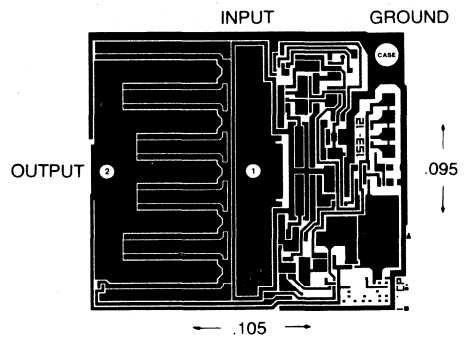
FEATURES

- **Load current in excess of 3A**
- **Output voltage trimmed to ±2%**
- **Complete self-contained protective features**
- **Correction for line resistance**
- **Eliminates external voltage setting resistors**
- **Hermetically sealed steel power package**
- **Available with 5, 8, 12, 15, and 18 volt outputs**

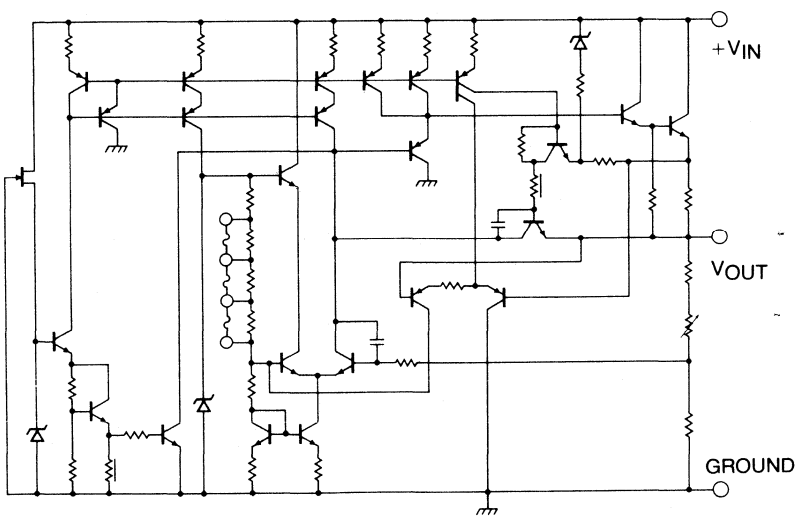
ABSOLUTE MAXIMUM RATINGS

Input Voltage	35 Volts
Power Dissipation (Internally limited)	50 Watts
Operating Temperature Range (T_J)	
SG153 Series	−55°C to +150°C
SG253 Series	−25°C to +150°C
SG353 Series	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

CHIP LAYOUT

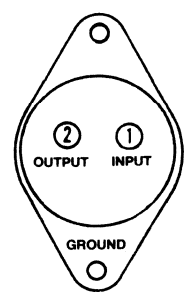


SIMPLIFIED SCHEMATIC



CONNECTION DIAGRAM

TOP VIEWS
(Case is internally connected to ground)



K-PACKAGE
TO-3

General-Purpose Positive Regulator

SG723/723C

This regulator is designed for use with either positive or negative supplies as a series, shunt, switching, or floating regulator with currents up to 150mA. Higher current requirements may be accommodated through the use of external NPN or PNP power transistors.

- **Positive or negative supply operation**
- **0.03% line and load regulation**
- **Output adjustable from 2 to 37V**
- **Low standby current drain**
- **0.002%/°C average temperature variation**

1

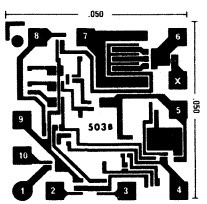
PARAMETERS	723[1]	723C[1]	UNITS
Operating Temperature Range	−55 to +125	0 to +70	°C
Package Types	T*, J	T*, J, N	—
Input Voltage Range	9.5 to 50	9.5 to 50	V
Output Voltage Range	2.0 to 37	2.0 to 37	V
Input/Output Differential	3.0 to 38	3.0 to 38	V
Load Regulation[2,3]	0.15	0.2	% V_{out}
Line Regulation V_{in} = 12 to 40V	0.2	0.5	% V_{out}
Ripple Rejection C_{ref} = 5μF; f = 50Hz to 10KHz	86 (typ)	86 (typ)	dB
Reference Voltage	6.95 – 7.35	6.80 – 7.50	V
Temperature Stability	0.015	0.015	%/°C
Output Noise Voltage C_{ref} = 0; BW = 100Hz to 10KHz	20 (typ)	20 (typ)	μV rms
Standby Current Drain	3.5	4.0	mA
Minimum Load Current	0	0	mA
Long Term Stability	0.1 (typ)	0.1 (typ)	%/khr

[1] Parameters apply at T_A = +25°C, except temperature stability is over temperature ranges.

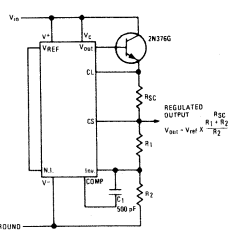
[2] Applies for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

[3] I_L = 1 to 50 mA.

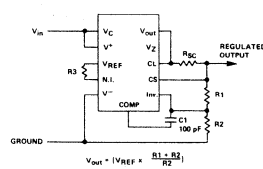
*T-package is TO-96 (can height: 240" max., 230" min.)



SG723/723C Chip
(See T-Package for pad functions)
Note: V_Z (Pin X) is available only in J or N-Package

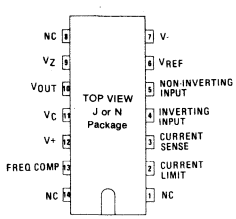


High Current Regulator
External NPN Transistor
I_L = 1A

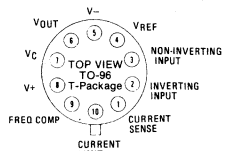


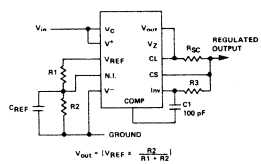
Basic High Voltage Regulator
V_{out} = 7 to 37 volts

CONNECTION DIAGRAMS



VZ available only in
J or N Package





Basic Low Voltage Regulator
V_{out} = 2 to 7 volts

SG1501A/2501A/3501A/4501

SG1501A dual tracking regulators are factory set to provide balanced ±15V outputs, but a single external adjustment can be used to change both outputs simultaneously. Line regulation of 20 mV and load regulation of 30 mV is guaranteed and, stability, over temperature, is 1% or less. Provision is made for adjustable current limiting and operation in excess of 2 amps is feasible with external transistors.

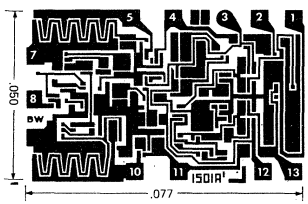
In the SG1501A, a built-in sensing circuit monitors junction temperature and shuts down the regulator above 170°C eliminating the need for concern about power dissipation under short circuit conditions. The SG1501A series also offers superior input/output voltage range and current handling capability (refer to table of specifications).

- **Thermal shutdown protection**
- **±35V inputs**
- **Output current to 200mA**
- **Output adjustable from ±10V to ±23V**

PARAMETERS[1]	1501A	2501A	3501A	4501	UNITS
Operating Temperature Range	−55 to +125	0 to +70	0 to +70	0 to +70	°C
Package Types	T, J		T,J,N		—
Output Voltage	±14.8/15.2		±14.5/15.5	±14.25/15.75	V
Input Voltage	±35		±30	±30	V
Input/Output Differential	2		2	2	V
Output Voltage Balance	150		300	300	mV
Line Regulation (V_{in} = 17 to V_{max})[5]	20		20	20	mV
Load Regulation (I_L = 0 to 50mA)[5]	30		30	30	mV
Output Voltage Range	10 to 23		10 to 23	10 to 23	V
Input Voltage Range ($8V_{out}$)	10 to 35		10 to 30	12 to 30[4]	V
Ripple Rejection (f = 120Hz)	75 (typ)		75 (typ)	75 (typ)	dB
Temperature Stability	1.0		1.0	1.0	%
Short Circuit Current Limit[2]	60 (typ)		60 (typ)	60 (typ)	mA
Output Noise Voltage[3]	50 (typ)		50 (typ)	50 (typ)	μVrms
Positive Standby Current	4		4	4	mA
Negative Standby Current	5		5	5	mA
Long Term Stability	0.1 (typ)		0.1 (typ)	0.1 (typ)	%/khr
Output Current	200		200	100	mA
Thermal Shutdown Protection	yes		yes	yes	—

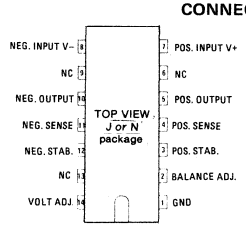
[1] All specifications apply to both positive and negative sides of the regulator, either singly or together. Unless otherwise specified T_A = +25°C, V_{in} = 20V, V_{out} = 15V, I_L = 0, Rsc = 0Ω, C1 = C2 = 0.01 mfd, C3 = C4 = 1.0 mfd, voltage adjust pin open

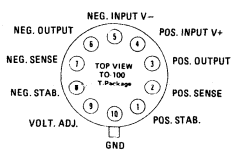
[2] Rsc = 10Ω [3] BW = 100Hz to 10kHz [4] 10V output [5] Over temperature range



SG1501A/2501A/3501A Chip (See T-package diagram for pad functions) Note: Balance Adjust (Pin X) is available only on D or N package.)

CONNECTION DIAGRAMS





See Applications Notes for additional information

SG1502/2502/3502

This circuit is identical to the SG1501 series of dual polarity tracking regulators except that the internal voltage setting resistors are not included and the current limit inputs have been disconnected from the pass transistors. While this circuit does require external divider resistors, maximum versatility is offered in adjusting the output voltage levels, and additional current-limit inputs ease the application of foldback current limiting. In all other respects, this circuit performs as the SG1501.

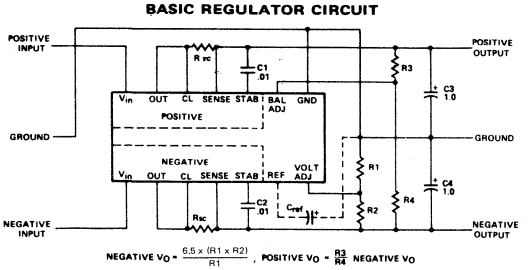
- **Positive and negative output voltages independently adjustable from 10 to 28V**
- **Output currents to 100mA**
- **Line and load regulation of 0.1%**
- **1% maximum temperature variation**
- **Standby current drain only 4mA**
- **Internal thermal shutdown protection**

PARAMETERS*	1502	2502	3502	UNITS
Operating Temperature Range	−55 to +125	0 to +70	0 to +70	°C
Package Types	J, N[4]		J, N	–
Input Voltage Range	±12/30		±12/25	V
Output Voltage Range	±10/28		±10/23	V
Input/Output Differential	2		2	V
Line Regulation (ΔV_{in} = 10V)[5]	0.2		0.2	% V_{out}
Load Regulation (I_L = 0 to 50mA)[5]	0.3		0.3	% V_{out}
Temperature Stability	1.0		1.0	% V_{out}
Current Limit Sense Voltage	0.6 (typ)		0.6 (typ)	V
Reference Voltage	6.3/6.6		6.2/6.8	V
Ripple Rejection f = 120Hz	75 (typ)		75 (typ)	dB
Output Noise Voltage[2]	50 (typ)		50	μVrms
Positive Standby Current[3]	4		4	mA
Negative Standby Current[3]	5		5	mA
Long Term Stability	0.1 (typ)		0.1 (typ)	%/khr

[1] All specifications apply to both positive and negative sides of the regulator either singly or together. Unless otherwise specified T_A = +25°C, V_{in} = +20V, V_{out} = +15V, I_L = 0, R_{SC} = 0Ω, C1 = C2 = 0.01 mfd, C3 = C4 = 1.0 mfd.

[2] BW = 100Hz to 10kHz [3] Divider 1 = 0.5mA [4] 1502 not available in plastic [5] Over temperature range

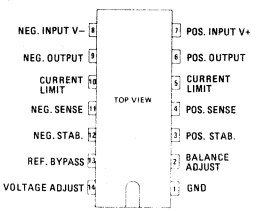
BASIC REGULATOR CIRCUIT

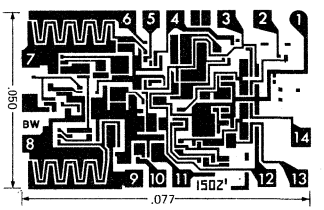


$$\text{NEGATIVE } V_O = \frac{6.5 \times (R1 \times R2)}{R1}, \quad \text{POSITIVE } V_O = \frac{R3}{R4} \text{ NEGATIVE } V_O$$

For best temperature performance, the parallel impedance of R1 and R2 should be 6.3 K ohm while that of R3 and R4 should be 10 K. Increasing the value of C1 and C2 will reduce the frequency response while transient response may be improved by increasing C3 and C4. For very low-noise applications, a 4.7 mfd capacitor for Cref may be added. Rsc is selected such that a sense voltage of 0.6 volts (at Tj = 25°C) is developed at the maximum load current desired.

CONNECTION DIAGRAM





See Applications Notes for additional information

PRECISION 2.5 VOLT REFERENCE

SG1503/SG2503/SG3503

1

DESCRIPTION

This monolithic integrated circuit is a fully self-contained precision voltage reference generator, internally trimmed for ±1% accuracy. Requiring less than 2 mA in quiescent current, this device can deliver in excess of 10 mA with total load and line induced tolerances of less than 0.5%. In addition to voltage accuracy, internal trimming achieves a temperature coefficient of output voltage of typically 10 ppm/°C. As a result, these references are excellent choices for application to critical instrumentation and D to A converter systems. The SG1503 is specified for operation over the full military temperature range of -55°C to +125°C, while the SG2503 and SG3503 are designed for commercial applications of 0°C to +70°C.

FEATURES

- **Output voltage trimmed to ±1%**
- **Input voltage range of 4.5 to 40V**
- **Temperature coefficient of 10 ppm/°C**
- **Quiescent current typically 1.5 mA**
- **Output current in excess of 10 mA**
- **Interchangeable with MC1503 and AD580**

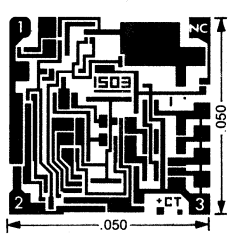
ABSOLUTE MAXIMUM RATINGS

Input Voltage	4.5 – 40V
Power Dissipation	600 mW
Derate Over 25°C	4.8 mW/°C

Operating Temperature Range	
SG1503	-55°C to +125°C
SG2503/3503	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

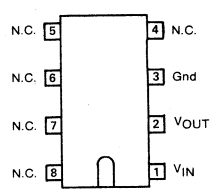
CONNECTION DIAGRAMS

CHIP LAYOUT

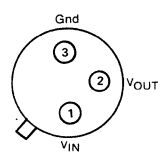


M or Y PACKAGE
MINIDIP

TOP VIEWS



T-PACKAGE
TO-39



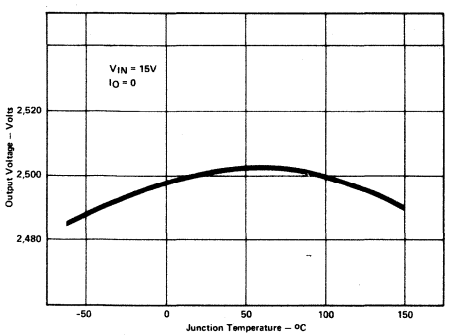
SG1503 / SG2503 / SG3503

ELECTRICAL CHARACTERISTICS

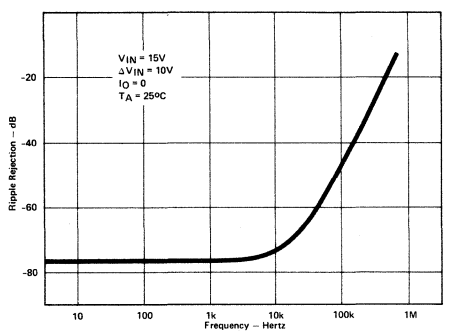
(Input Voltage = 15V, I_L = 0 mA, T_A = Operating Temperature Range unless otherwise stated.)

PARAMETER	TEST CONDITIONS	SG1503/2503			SG3503			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	T_A = 25°C	2.485	2.50	2.515	2.475	2.50	2.525	Volts
Input Voltage Range	T_A = 25°C	4.5	—	40	4.5	—	40	Volts
Input Voltage Range	Over Operating Temperature	4.7	—	40	4.7	—	40	Volts
Line Regulation	V_{IN} = 5 to 15V	—	1	3	—	1	3	mV
Line Regulation	V_{IN} = 15 to 40V	—	3	5	—	3	10	mV
Load Regulation	ΔI_L = 10 mA	—	3	5	—	3	10	mV
Load Regulation	ΔI_L = 10 mA, V_{IN} = 30V	—	4	8	—	4	15	mV
Temperature Regulation	-55° to +125°C	—	15	20	—	—	—	mV
Temperature Regulation	0°C to +70°C	—	2.5	5	—	5	10	mV
Quiescent Current	V_{IN} = 40V	—	1.5	2.0	—	1.5	2.0	mA
Short Circuit Current		15	20	30	15	20	30	mA
Ripple Rejection	f = 120 Hz, T_A = 25°C	—	76	—	—	76	—	dB
Output Noise	B.W. = 10 kHz, T_A = 25°C	—	100	—	—	100	—	μV_{rms}
Stability		—	250	—	—	250	—	$\mu V/kHr$

OUTPUT VOLTAGE vs. TEMPERATURE



RIPPLE REJECTION



SG1511 / SG3511

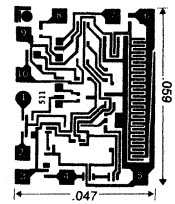
Description

This monolithic voltage regulator is designed for negative applications as a complement to the popular SG723 positive regulator and has the same high degree of versatility, and wide range of applications. The SG1511/3511 regulator consists of a temperature compensated reference, error amplifier, series pass transistor, temperature compensated, low-threshold current limit and remote shutdown circuitry. This device by itself will supply load currents of up to 50mA with higher current requirements easily accommodated through the use of external NPN or PNP power transistors.

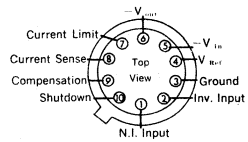
The SG1511 is specified to operate over the full military temperature range of −55°C to +125°C while the SG3511 is designed for commercial applications of 0°C to +70°C.

Absolute Maximum Ratings

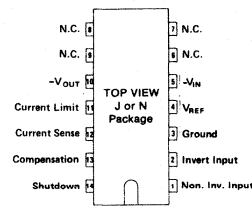
Input voltage	−40 volts
Input-output voltage differential	−40 volts
Maximum output current	−50mA
Current from V_{REF}	− 5mA
Power dissipation	680mW
Derate above 25°C	5.4 mW/°C
Operating temperature range	−55°C to +125°C
Storage temperature range	−65°C to +150°C



CONNECTION DIAGRAMS



Note: Pin 5 is connected to case.



Features

- **Output adjustable from −2 to −37 volts**
- **Output current to 50mA**
- **.002%/°C average temperature variation**
- **Temperature compensated current limiting**
- **.03% line and load regulation**

Electrical Characteristics Unless otherwise specified, $T_A = 25°C$, $V_{in} = -12V$, $V_O = -5V$, $I_L = 1mA$, $R_{SC} = 0\Omega$, $C = 2200$ pf, $R_{SD} = 0\Omega$.

Parameters	Conditions	Min.	Typ.	Max.	Units
Input Voltage Range		−9.5		−40	V
Output Voltage Range		−2.0		−37	V
Input-Output Differential		−3.0		−38	V
Line Regulation	V_{in} = −9 to −12V		.01	0.1	% V_O
	V_{in} = −12 to −40V		.02	0.2	% V_O
Load Regulation	I_L = 1 to 20mA		.03	0.1	% V_O
Ripple Rejection	f = 50 Hz to 10 kHz		86		db
Temperature Stability	Over Operating Range		.002	.015	%/°C
Current Limit Sense Voltage			70		mV
Current Limit T_C			±0.2		mV/°C
Reference Voltage		−5.9	−6.2	−6.5	V
Shutdown Resistance (R_{SD})		2.0	3.0	5.0	K ohm
Standby Current Drain	V_{in} = −30V		1.5	2.5	mA
Output Noise Voltage	BW = 100Hz to 10KHz		20		μV_{rms}
Long Term Stability			0.1		%/Khr.

Applications

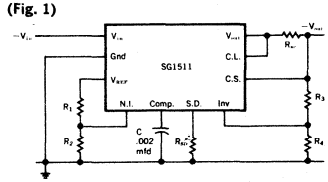
Basic Negative Voltage Regulator (Fig. 1)

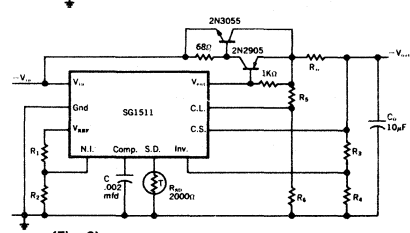
1. For low voltage applications, ($V_O = -2$ to $-6V$):
$$V_O = \frac{V_{REF}\,R_2}{R_1 + R_2}, \quad R_3 = \frac{R_1\,R_2}{R_1 + R_2},$$
$$\frac{V_{REF}}{R_1 + R_2} < 500\,\mu A, \quad R_4 = \infty$$
2. For high voltage application, ($V_O = -6$ to $-37V$)
$$V_O = \frac{V_{REF}\,(R_3 + R_4)}{R_4}, \quad R_1 = \frac{R_3\,R_4}{R_3 + R_4}, \quad R_2 = \infty$$
3. For constant-current limiting:
$$R_{sc} = \frac{70\text{ mV}}{I_{sc}\text{ (max)}}$$
4. If shut-down is not required, set $R_{SD} = 0$.
Regulator will shut-down when $R_{SD} > 5K$ ohms.

High Current Applications (Fig. 2)

1. Select R_1, R_2, R_3 and R_4 as per basic regulator application.
2. For thermal shutdown, mount thermistor R_{SD} with close thermal coupling to the 2N3055 power transistor.
3. R_5 and R_6 provide foldback current limiting:
$$I_{sc} = \frac{70mV}{R_{sc}}, \quad I_{max} = \frac{70mV}{R_{sc}} + \frac{V_O\,R_5}{R_{sc}\cdot(R_5 + R_6)}$$

(Fig. 1)





(Fig. 2)

SG1524 / SG2524 / SG3524

Description

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG1524 is specified for operation over the full military temperature range of −55°C to +125°C, while the SG2524 and SG3524 are designed for commercial applications of 0°C to +70°C.

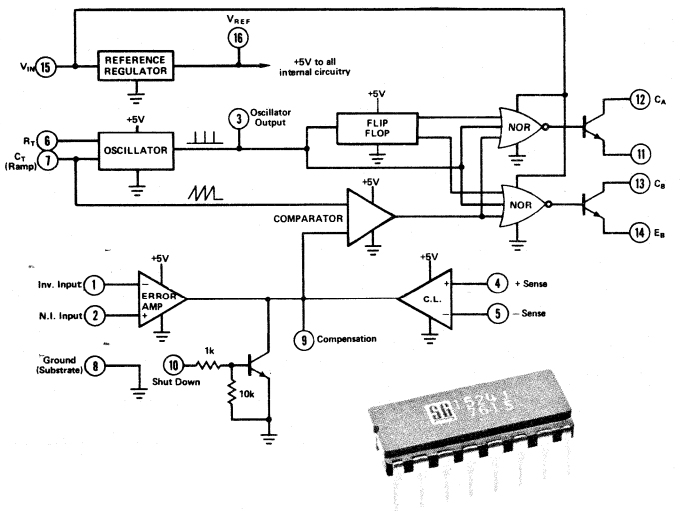
Features

- Complete PWM power control circuitry
- Single ended or push-pull outputs
- Line and load regulation of 0.2%
- 1% maximum temperature variation
- Total supply current less than 10mA
- Operation beyond 100kHz

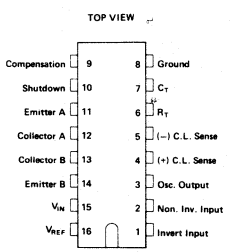
Absolute Maximum Ratings

Input Voltage	40V
Output Current (each output)	100mA
Reference Output Current	50mA
Oscillator Charging Current	5mA
Power Dissipation (package limitation)	1000mW
Derate above 25°C	8mW/°C
Operating Temperature Range	
SG1524	−55°C to +125°C
SG2524/SG3524	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

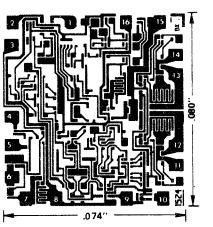
BLOCK DIAGRAM



CONNECTION DIAGRAM



CHIP LAYOUT

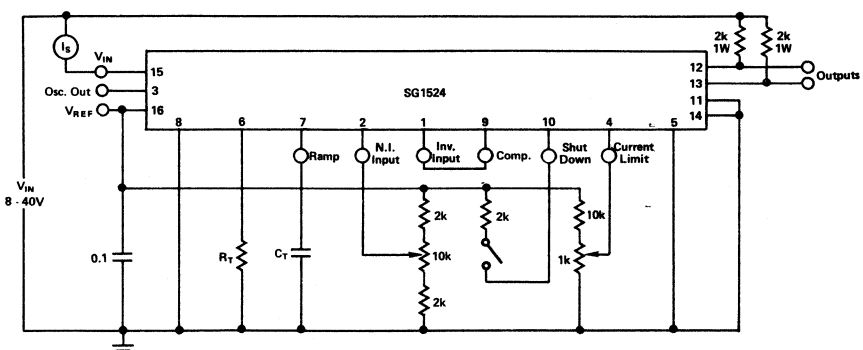


SG1524 / SG2524 / SG3524

Electrical Characteristics (Unless otherwise stated, these specifications apply for T_A= −55°C to +125°C for the SG1524 and 0°C to +70°C for the SG2524 and SG3524, V_{IN}= 20V, and f = 20kHz)

PARAMETER	CONDITIONS	SG1524		SG2524	SG3524			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section:								
Output Voltage:		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	V_{IN} = 8 to 40 Volts	–	10	20	–	10	30	mV
Load Regulation	I_L = 0 to 20mA	–	20	50	–	20	50	mV
Ripple Rejection	f = 120 Hz, T_A = 25°C	–	66	–	–	66	–	dB
Short Circuit Current Limit	V_{REF} = 0, T_A = 25°C	–	100	–	–	100	–	mA
Temperature Stability	Over Operating Temperature Range	–	0.3	1	–	0.3	1	%
Long Term Stability	T_A = 25°C	–	20	–	–	20	–	mV/khr
Oscillator Section:								
Maximum Frequency	C_T = .001 mfd, R_T = 2kΩ	–	300	–	–	300	–	kHz
Initial Accuracy	R_T and C_T constant	–	5	–	–	5	–	%
Voltage Stability	V_{IN} = 8 to 40 Volts, T_A = 25°C	–	–	1	–	–	1	%
Temperature Stability	Over Operating Temperature Range	–	–	2	–	–	2	%
Output Amplitude	Pin 3, T_A = 25°C	–	3.5	–	–	3.5	–	V
Output Pulse Width	C_T = .01 mfd, T_A = 25°C	–	0.5	–	–	0.5	–	μS
Error Amplifier Section:								
Input Offset Voltage	V_{CM} = 2.5 Volts	–	0.5	5	–	2	10	mV
Input Bias Current	V_{CM} = 2.5 Volts	–	2	10	–	2	10	μA
Open Loop Voltage Gain		72	80	–	60	80	–	dB
Common Mode Voltage	T_A = 25°C	1.8	–	3.4	1.8	–	3.4	V
Common Mode Rejection Ratio	T_A =25°C	–	70	–	–	70	–	dB
Small Signal Bandwidth	A_V = 0dB, T_A = 25°C	–	3	–	–	3	–	MHz
Output Voltage	T_A = 25°C	0.5	–	3.8	0.5	–	3.8	V
Comparator Section:								
Duty Cycle	% Each Output On	0	–	45	0	–	45	%
Input Threshold	Zero Duty Cycle	–	1	–	–	1	–	V
Input Threshold	Max. Duty Cycle	–	3.5	–	–	3.5	–	V
Input Bias Current		–	1	–	–	1	–	μA
Current Limiting Section:	Pin 9 = 2V with Error Amplifier Set for Max Out, T_A = 25°C							
Sense Voltage		190	200	210	180	200	220	mV
Sense Voltage T.C.		–	0.2	–	–	0.2	–	mV/°C
Common Mode Voltage		−1	–	+1	−1	–	+1	V
Output Section: (Each Output)								
Collector-Emitter Voltage		40	–	–	40	–	–	V
Collector Leakage Current	V_{CE} = 40V	–	0.1	50	–	0.1	50	μA
Saturation Voltage	I_C = 50mA	–	1	2	–	1	2	V
Emitter Output Voltage	V_{IN} = 20V	17	18	–	17	18	–	V
Rise Time	R_C = 2K ohm, T_A = 25°C	–	0.2	–	–	0.2	–	μS
Fall Time	R_C = 2K ohm, T_A = 25°C	–	0.1	–	–	0.1	–	μS
Total Standby Current: (Excluding oscillator charging current, error and current limit dividers, and with outputs open)	V_{IN} = 40V	–	8	10	–	8	10	mA

OPEN LOOP TEST CIRCUIT



SG1524 / SG2524 / SG3524

Oscillator

The oscillator in the SG1524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to $3.6V \div R_T$ and should be kept within the range of approximately 30 μA to 2 mA, i.e., $1.8k < R_T < 100k$. The range of values for C_T also has limits as the discharge time of C_T determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 1. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing the blanking pulse prior to the flip-flop's reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance ($\approx$ 100 pf) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 1.0 mfd.

The oscillator period is approximately $t = R_T C_T$ where t is in microseconds when R_T = ohms and C_T = microfarads.

The use of Figure 2 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0 - 90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each output's duty cycle is 0 - 45% and the overall frequency is ½ that of the oscillator.

If it is desired to synchronize the SG1524 to an external clock, a pulse of $\approx$ + 3 volts may be applied to the oscillator output terminal with $R_T C_T$ set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2k ohms.

If two or more SG1524's must be synchronized together, the easiest method is to interconnect all pin 3 terminals, tie all pin 7's together and to a single C_T, leave all pin 6's open except one which is connected to a single R_T.

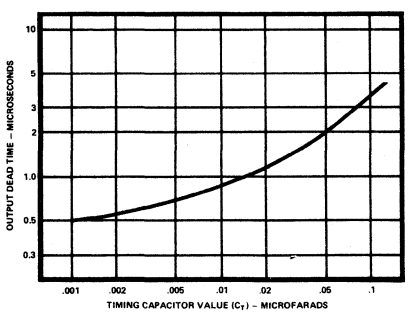


FIGURE 1. Output stage dead time as a function of the timing capacitor value.

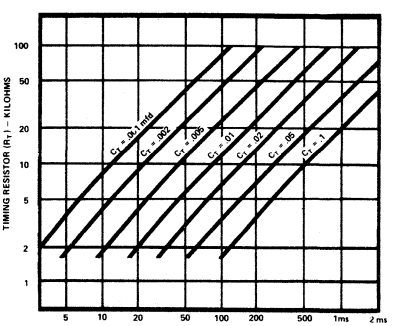


FIGURE 2. Oscillator period as a function of R_T and C_T.

SG1524 / SG2524 / SG3524

Current Limiting

The current limiting circuitry of the SG1524 is shown in Figure 3.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R_1,

$$\text{Threshold} = V_{BE}\ (Q1) + I_1 R_2 - V_{BE}\ (Q2) = I_1 R_2$$
$$\approx 200\,mV$$

Although this curcuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300 Hertz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

If this current limit circuitry is unused, pins 4 and 5 should both be grounded.

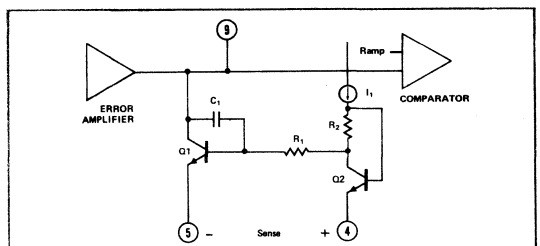
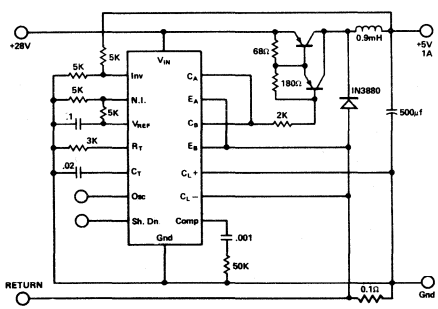
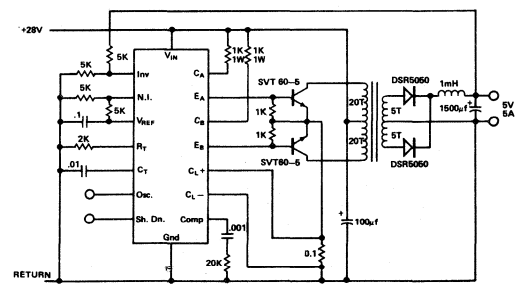


FIGURE 3. Current Limiting Circuitry of the SG1524.



In this conventional single-ended regulator circuit, the two outputs of the SG1524 are connected in parallel for effective 0 - 90% duty-cycle modulation. The use of an output inductor requires and R-C phase compensation network for loop stability.



Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the SG1524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

REGULATING PULSE WIDTH MODULATORS

SG1525/2525/3525
SG1527/2527/3527

ADVANCED DATA
Performance data described herein represent design goals.
Final device specifications are subject to change.

1

DESCRIPTION

The SG1525/1527 series of pulse width modulator integrated circuits are designed to offer improved reference accuracy and lowered external parts count when used to implement switching power supplies. The on-chip +5.1 volt reference is trimmed to ±1% initial accuracy; and the common mode range of the error amplifier includes the reference voltage, eliminating external divider resistors. A Sync input to the oscillator allows multiple units to be slaved together, or for a single unit to be synchronized to an external system clock. A single resistor between the C_T pin and the Discharge pin provides a wide range of deadtime adjustment. These devices also feature internal clamp diodes and current sources for soft-start. A timing capacitor is the only external component required. A Shutdown pin controls the soft-start circuitry, allowing external monitoring devices to initiate soft-start cycles. The output stages are totem-pole designs capable of sourcing or sinking 100mA. The SG1525 output stage features NOR logic, giving a normally LOW output level. The SG1527 utilizes OR logic, which results in a normally HIGH output level. The SG1500 series parts are specified for operation over the full military temperature range of −55°C to +125°C. The SG2500 series parts are designed for the industrial temperature range of −25°C to +85°C. The SG3500 series parts are characterized for the commercial temperature range of 0°C to +70°C.

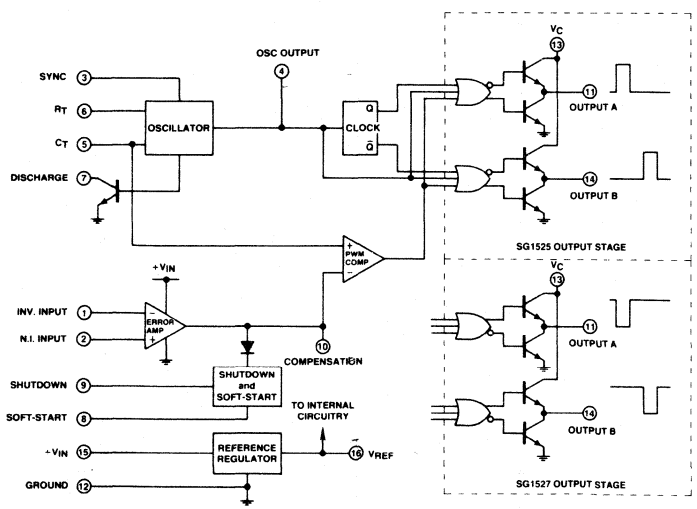
FEATURES

- 8 to 40 VOLT OPERATION
- 5.1 VOLT REFERENCE TRIMMED TO ±1%
- ADJUSTABLE DEADTIME
- INTERNAL SOFT-START
- 5.1 VOLT ERROR AMP COMMON MODE INPUT
- DUAL 100mA SOURCE/SINK OUTPUT DRIVERS
- OSCILLATOR SYNC TERMINAL

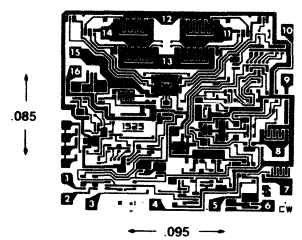
ORDER INFORMATION

Package	Temperature Range	Part Number
16-pin Ceramic DIP	−55°C to +125°C	SG1525J/SG1527J
16-pin Ceramic DIP	−25°C to +85°C	SG2525J/SG2527J
16-pin Ceramic DIP	0°C to +70°C	SG3525J/SG3527J
Dice	−55°C to +125°C	Consult Factory
Dice	0°C to +70°C	Consult Factory

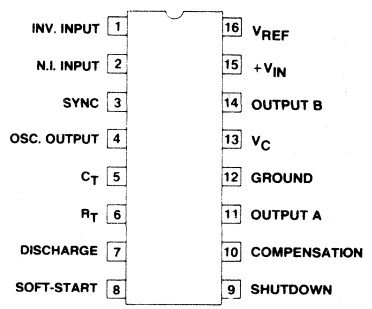
BLOCK DIAGRAM



CHIP LAYOUT



CONNECTION DIAGRAM
TOP VIEW



J-PACKAGE
TO-116

SG1525/2525/3525
SG1527/2527/3527

ADVANCED DATA

Performance data described herein represent design goals.
Final device specifications are subject to change.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+Vin)	40 Volts	Derate above 50°C	10mW/°C
Output Collector Voltage (V_C)	60 Volts	Operating Ambient Temperature Range	
Output Current, Source or Sink	200 mA	SG1525, SG1527	−55°C to +125°C
Reference Output Current	50 mA	SG2525, SG2527	−25°C to +85°C
Oscillator Charging Current	5 mA	SG3525, SG3527	0°C to +70°C
Power Dissipation	1000mW	Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS:

Note: These specifications apply for the specified operating temperature range, Vin = 20V, R_T = 2kΩ, C_T = .01mF; R_{DB} = 0Ω, unless otherwise specified.

		SG1525/2525 SG1527/2527			SG3525 SG3527			
Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Units
REFERENCE SECTION								
Output Voltage	T_J = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	Vin = 8 to 30V		10	20		10	20	mV
Load Regulation	I_L = 0 to 20mA		20	40		20	50	mV
Temp Regulation	Over Operating Temp Range		20	50		20	50	mV
Total Output Variation	Line, Load & Temp	5.00		5.20	4.95		5.25	V
Short Circuit Current	V_{REF} = 0, T_J = 25°C		80	100		80	100	mA
Output Noise Voltage	10Hz≤f≤10kHz.T_J = 25°C		40			40		μVrms
Long Term Stability	T_J = 125°C		20			20		mV/khr
OSCILLATOR SECTION								
Maximum Freq.	R_T = 2kΩ,C_T= .001mF	300			300			kHz
Initial Accuracy			±5			±5		%
Voltage Stability	Vin = 8 to 30V		±1			±1		%
Temperature Stability	Over Operating Temp Range		±2			±2		%
Clock Amplitude	C_T = .01mF	3.0	3.5		3.0	3.5		V
Clock Width	C_T = .01mF		0.5			0.5		μsec
Sync Threshold			1.0	2.0		1.0	2.0	V
Sync Input Current	Sync Voltage = 3.5V		0.2	0.4		0.2	0.4	mA
Sawtooth Valley Voltage		0.6	1.0		0.6	1.0		V
Current Mirror	I_{RT} = 2mA	1.8	2.0	2.2	1.8	2.0	2.2	mA
ERROR AMPLIFIER SECTION								
Input Offset Voltage	V_{CM}= 5.1V		0.5	5		2	10	mV
Input Bias Current			1	10		1	10	μA
Input Offset Current				1			1	μA
CMRR	V_{CM}= 2 to 12 Volts	60	72		60	72		dB
PSRR	Vin = 8 to 30 Volts	50	60		50	60		dB
Output Low Level				0.5			0.5	V
Output High Level		3.8			3.8			V
Open Loop Gain	R_L = 10 MegΩ	60	72		60	72		dB
Bandwidth			2			2		MHz
COMPARATOR SECTION								
Min. Duty Cycle				0			0	%
Max. Duty Cycle		45		49	45		49	%
Input Threshold	Zero Duty Cycle		1.0			1.0		V
Input Threshold	Max. Duty Cycle		3.3			3.3		V
Input Bias Current			1.0			1.0		μA
SHUTDOWN SECTION								
Soft Start Current	V_{SD} = 0V	50	100	175	50	100	175	μA
Soft Start Voltage	V_{SD} =2V			0.15			0.15	V
Error Clamp Voltage	V_{SD} =2V			0.15			0.15	V
Input Current	V_{SD} =2V			3			3	mA
OUTPUT SECTION								
Output Low Level	Isink = 20mA		0.2	0.4		0.2	0.4	V
	Isink = 100mA		1.0	2.0		1.0	2.0	V
Output High Level	Isource = 20mA			18			18	V
	Isource = 100mA			17			17	V
Collector Leakage	V_C= 50V (Note 1)			100			100	μA
Rise Time			100			100		nsec
Fall Time			100			100		nsec
Shutdown Delay Time	V_{SD} =2V		1			1		μsec
TOTAL STANDBY CURRENT								
	Vin = 30V. Shutdown = 2V		14	20		14	20	mA

Note 1. Applies to SG1525/2525/3525 only.

REGULATING PULSE WIDTH MODULATOR

SG1526/SG2526/SG3526

ADVANCED DATA

SG1526/SG2526/SG3526

Performance data described herein represent design goals.
Final device specifications are subject to change.

1

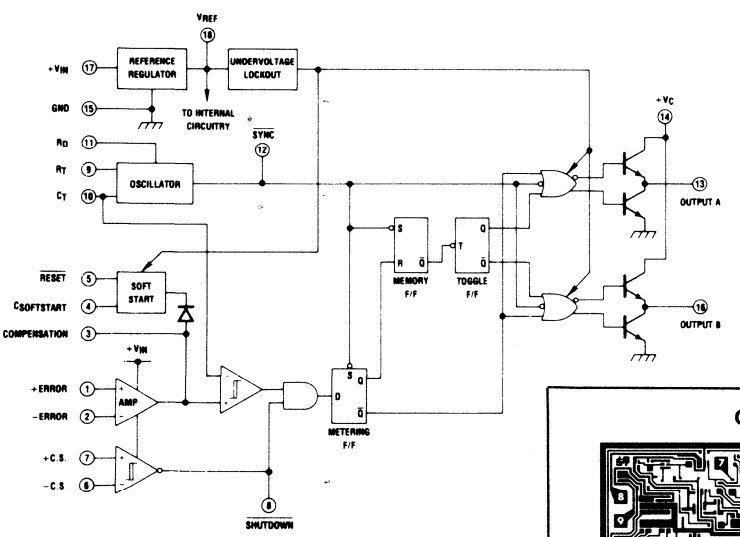
DESCRIPTION

The 1526 is a high performance monolithic pulse width modulator circuit designed for fixed-frequency switching regulators and other power control applications. Included in an 18-pin dual-in-line package are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two low impedance power drivers. Also included are protective features such as soft-start and undervoltage lockout, digital current limiting, double pulse inhibit, frequency limiting, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The SG1526 is characterized for operation over the full military junction temperature range of −55°C to +150°C. The SG2526 is characterized for operation from −25°C to +150°C, and the SG3526 is characterized for operation from 0°C to +125°C.

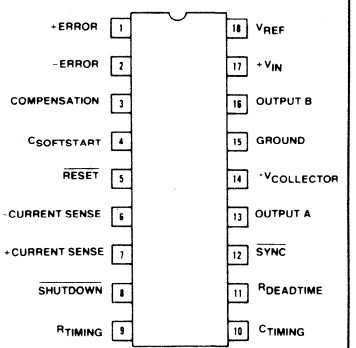
FEATURES

- 8 TO 40 VOLT OPERATION
- 5 VOLT REFERENCE TRIMMED TO ±1%
- 50 HZ TO 300 KHZ OSCILLATOR RANGE
- DUAL 100 MA SOURCE/SINK OUTPUTS
- DIGITAL CURRENT LIMITING
- DOUBLE PULSE SUPRESSION
- PROGRAMMABLE DEADTIME
- UNDERVOLTAGE LOCKOUT
- PULSE METERING FOR FREQUENCY LIMITING
- PROGRAMMABLE SOFT-START
- HIGH CURRENT LIMIT COMMON MODE RANGE
- HIGH ERROR AMP COMMON MODE RANGE
- TTL/CMOS COMPATIBLE LOGIC PORTS
- SYMMETRY CORRECTION CAPABILILITY
- GUARANTEED 6 UNIT SYNCHRONIZATION

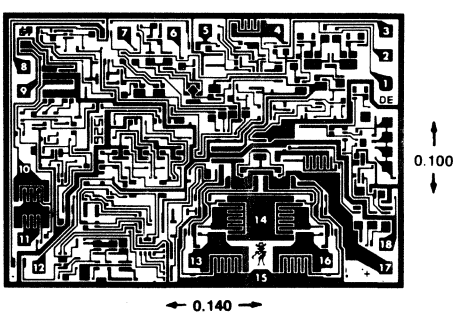
BLOCK DIAGRAM



CONNECTION DIAGRAM



CHIP LAYOUT



SG1526/SG2526/SG3526

ADVANCED DATA

Performance data described herein represent design goals.
Final device specifications are subject to change.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage	+45V	Power Dissipation at T_A = +25°C (Note 2)	1000mW
Collector Supply Voltage	+60V	Thermal Resistance: junction to ambient	125°C/W
Logic Inputs	−0.3V to +5.5V	Power Dissipation at T_C = +25°C (Note 3)	3000mW
Analog Inputs	−0.3V to +Vin	Thermal Resistance: junction to case	42°C/W
Source/Sink Load Current (each output)	200mA	Operating Junction Temperature	+150°C
Reference Load Current	50mA	Storage Temperature Range	−65°C to +150°C
Logic Sink Current	15mA	Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1. Values beyond which damage may occur.
Note 2. Derate at 8mW/°C for ambient temperatures above +25°C.
Note 3. Derate at 24mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage	+8V to +40V	Oscillator Timing Capacitor	1nF to 10μF
Collector Supply Voltage	+5V to +50V	Programmed Deadtime Range	3% to 50%
Sink/Source Load Current (each output)	0 to 100mA	Operating Junction Temperature Range	
Reference Load Current	0 to 20mA	SG1526	−55°C to +150°C
Oscillator Frequency Range	50Hz to 300kHz	SG2526	−25°C to +150°C
Oscillator Timing Resistor	2kΩ to 150kΩ	SG3526	0°C to +125°C

Note 4. Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL CHARACTERISTICS (+Vin = 15V, and over operating temperature, unless otherwise specified)

PARAMETER	CONDITIONS	SG1526/2526/3526 MIN	SG1526/2526/3526 TYP	SG1526/2526/3526 MAX	UNITS
REFERENCE SECTION (Note 5)					
Output Voltage	T_J = +25°C	4.95	5.00	5.05	V
Line Regulation	+Vin = 8 to 40 V		10		mV
Load Regulation	I_L = 0 to 20 mA		10		mV
Temperature Stability	Over Operating T_J		15		mV
Total Output Voltage Range	Over Recommended Operating Conditions		5.00		V
Short Circuit Current	V_{REF} = 0V		50		mA
OSCILLATOR SECTION (Note 6)					
Initial Accuracy	T_J = +25°C		3		%
Voltage Stability	+Vin = 8 to 40 V		0.5		%
Temperature Stability	Over Operating T_J		1		%
Total Oscillator Frequency Stability	Over Recommended Operating Conditions		2		%
Minimum Frequency	R_T = 150 kΩ, C_T = 10μF			50	Hz
Maximum Frequency	R_T = 2 kΩ, C_T = 1.0nF	300			kHz
Sawtooth Peak Voltage	+Vin = 40V		3.0		V
Sawtooth Valley Voltage	+Vin = 8 V		1.0		V
$\overline{SYNC}$ Pulsewidth	C_L = 15pF		0.5		μsec

Note 5. I_L = 1mA.
Note 6. F = 40kHz (R_T = 3.65kΩ ±1%, C_T = .01μF ±1%, R_D = 0Ω).

ELECTRICAL CHARACTERISTICS (continued)

PARAMETERS	CONDITIONS	SG1526/2526/3526			UNITS
		MIN	TYP	MAX	
ERROR AMPLIFIER SECTION (Note 7)					
Input Offset Voltage	$R_S \leq 2\ k\Omega$		2		mV
Input Bias Current			−350		nA
Input Offset Current			35		nA
DC Open Loop Gain	$R_L \geq 10\ Meg\Omega$		75		dB
Open Loop Bandwidth	C_L = 15pF	1			MHz
Output Voltage Swing Vout High Vout Low	 $R_L \geq 50\ k\Omega$ $R_L \geq 50\ k\Omega$		 4.2 0.1		 V V
Common Mode Range	+Vin = 8 V	0		5.2	V
Common Mode Rejection	$R_S \leq 10\ k\Omega$		72		dB
Supply Voltage Rejection	F = 120 Hz, ΔVin = 1V		80		dB
DIGITAL PORTS (SYNC, SHUTDOWN, and RESET)					
HIGH Output Voltage	Isource = 40μA	2.4	4.0		V
LOW Output Voltage	Isink = 3.6 mA		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4 V		−125	−200	μA
LOW Input Current	V_{IL} = +0.4 V		−225	−360	μA
CURRENT LIMIT COMPARATOR					
Common Mode Range	+Vin = 40 V	0		37	V
Sense Voltage	V_{CM} = 0 to 37 V		100		mV
Input Bias Current	V_{CM} = 0 to 37 V		−3		μA
Voltage Gain	$\overline{SHUTDOWN}$ Isink = 360μA		68		dB
Response Time to Output Driver	100 mV Step, 5 mV Over-drive, $R_{source} \leq 50\ \Omega$		0.3		μsec
SOFT—START SECTION					
Error Clamp Voltage	$\overline{RESET}$ = +0.4 V		0.1		V
C_S Charging Current	$\overline{RESET}$ = +2.4 V		100		μA
OUTPUT DRIVERS (Each Output) (Note 8)					
HIGH Output Voltage	I_{source} = 20 mA		13.5		V
	I_{source} = 100 mA		13		V
LOW Output Voltage	Isink = 20 mA		0.2		V
	Isink = 100 mA		1.2		V
Collector Leakage	V_C = 50 V		0.1		μA
Rise Time	C_L = 1000 pF		0.3		μsec
Fall Time	C_L = 1000 pF		0.2		μsec
POWER CONSUMPTION (Note 9)					
Standby Current	$\overline{SHUTDOWN}$ = +0.4 V		30		mA

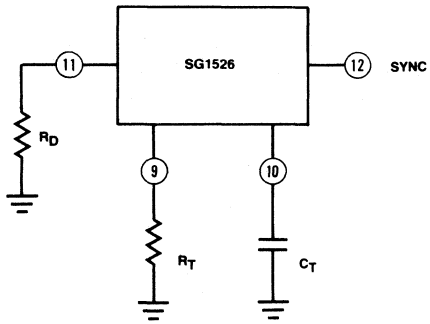
Note 7. V_{CM} = 0 to 5.2 V
Note 8. Vcollector = +15 V, Rcollector = 0Ω
Note 9. +Vin = 40 V, R_T = 3.6 kΩ

SG1526/SG2526/SG3526

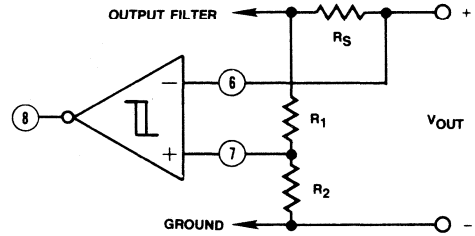
ADVANCED DATA

Performance data described herein represent design goals.
Final device specifications are subject to change.

OSCILLATOR CONNECTIONS

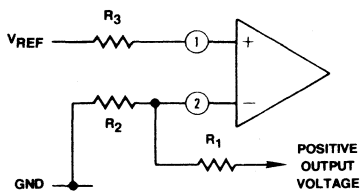


FOLDBACK CURRENT LIMITING



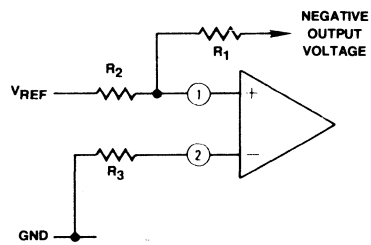
$$I_{MAX} = \frac{0.1V + \left(\frac{V_{OUT}\,R_1}{R_1+R_2}\right)}{R_S} \qquad I_{SC} = \left(\frac{0.1V}{R_S}\right)$$

ERROR AMPLIFIER CONNECTIONS



$$V_{OUT} = V_{REF}\left(\frac{R_1 + R_2}{R_2}\right)$$

$$R_3 = \left(\frac{R_1R_2}{R_1+R_2}\right)$$



$$V_{OUT} = V_{REF}\left(\frac{R_1}{R_2}\right)$$

$$R_3 = \left(\frac{R_1R_2}{R_1+R_2}\right)$$

DRIVING VMOS POWER FETS

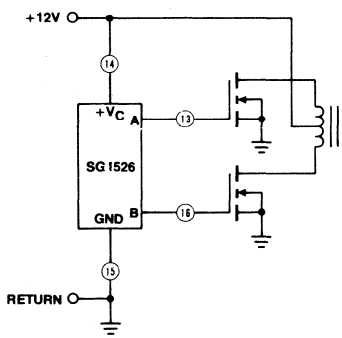


Figure 1. The totem-pole output drivers of the SG1526 are ideally suited for driving the input capacitance of power FETs at high speeds.

FLYBACK CONVERTER WITH CURRENT LIMITING

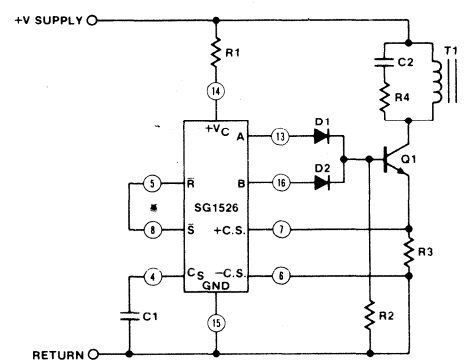


Figure 2. In this circuit, current limiting is accomplished by using the current limit comparator output to reset the soft-start capacitor.

SG1532 / SG2532 / SG3532

DESCRIPTION

This monolithic integrated circuit is a versatile, general-purpose voltage regulator designed as a substantially improved replacement for the popular SG723 device. The SG1532 series regulators retain all the versatility of the SG723 but have the added benefits of operation with input voltages as low as 4.5 volts and as high as 50 volts; a low noise, low voltage reference; temperature compensated, low threshold current limiting; and protective circuits which include thermal shutdown and independent current limiting of both the reference and output voltages. Also included is a separate remote shutdown terminal and – in the dual-in-line package – open collector outputs for low input-output differential applications.

These devices are available in both hermetic 14-pin cerdip DIL and 10-pin TO-96 packages. In the T-package, these units are interchangeable with the LAS-1000 and LAS-1100 regulators. The SG1532 is rated for operation over the temperature range of -55°C to +125°C while the SG2532 and SG3532 are intended for industrial applications of 0°C to +70°C.

FEATURES:

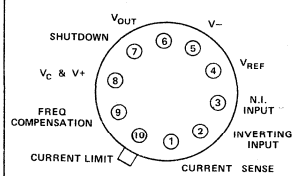
- **Input voltage range of 4.5 to 50 volts**
- **2.5 volt low noise reference**
- **Independent shutdown terminal**
- **Improved line and load regulation**
- **80 mV current limit sense voltage**
- **Fully protected including thermal shutdown**
- **Useful output current to 150 mA**

ABSOLUTE MAXIMUM RATINGS:

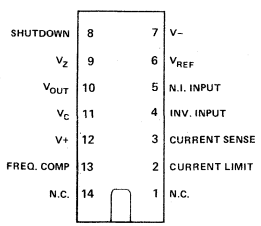
Input Voltage	
SG1532/2532	50 Volts
SG3532	40 Volts
Output Current	250 mA
Reference Current	25 mA
Zener current (J-package only)	25 mA
Storage Temperature Range	-65°C to +150°C
Power Dissipation	
T-Package (TO-96)	800 mW
Derate Above 25°C	6.4 mW/°C
J-Package (TO-116)	1000 mW
Derate Above 25°C	8 mW/°C
Operating Temperature Range	
SG1532	-55°C to +125°C
SG2532 and SG3532	0°C to +70°C

CONNECTION DIAGRAMS

TOP VIEWS

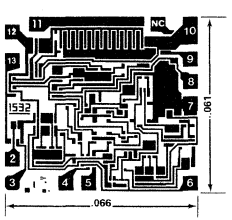


T-Package (TO-96)



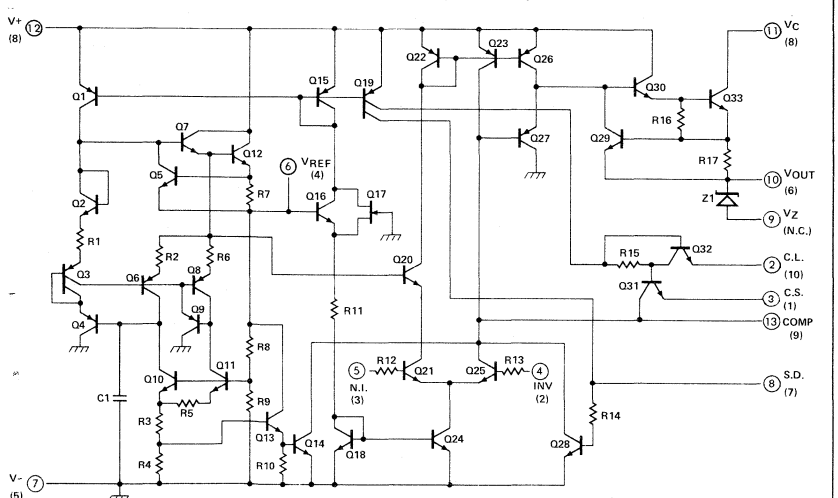
J-Package (TO-116)

CHIP LAYOUT (J-pkg)



SIMPLIFIED SCHEMATIC

Pins numbered for J-Package – T-Package numbers in parenthesis



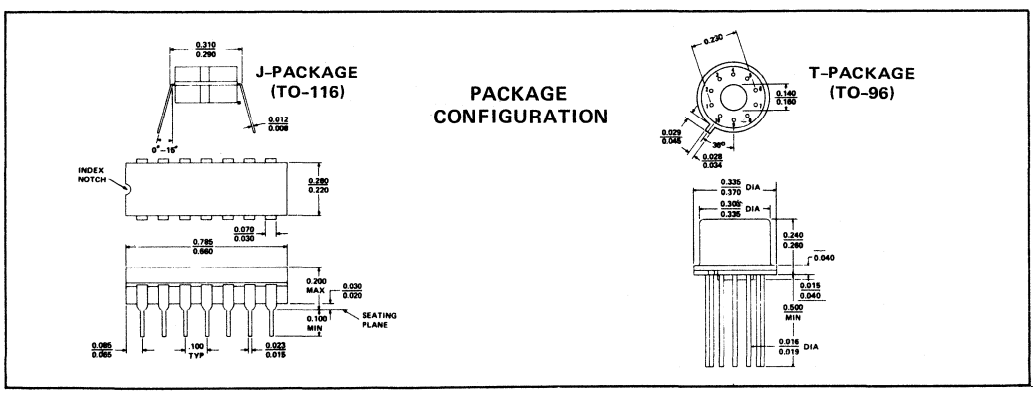
SG1532 / SG2532 / SG3532

ELECTRICAL CHARACTERISTICS (See Notes 1 & 2)

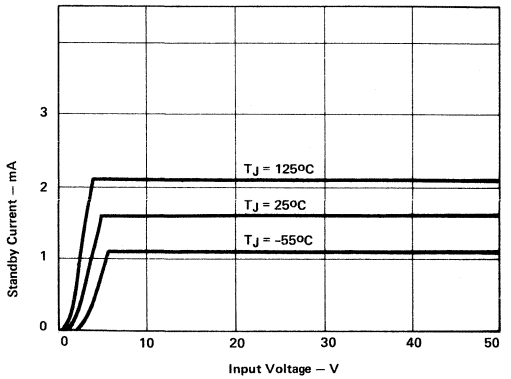
PARAMETER	CONDITIONS	SG1532/2532			SG3532			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage	T_A = 25°C	4.5	–	50	4.5	–	40	Volts
Input Voltage	Over Temperature Range	4.7	–	50	4.7	–	40	Volts
Output Voltage		2.0	–	38	2.0	–	38	Volts
Max Output Current	R_{SC} = 0, V_O = 0, T_A = 25°C	–	175	250	–	175	250	mA
Min (V_{IN} - V_O)	I_O = 100 mA, T_A = 25°C	–	1.7	2.0	–	1.7	2.0	Volts
Reference Voltage	T_A = 25°C	2.40	2.50	2.60	2.40	2.50	2.60	Volts
Reference Voltage	Over Temperature Range	2.35	–	2.65	2.35	–	2.65	Volts
Temperature Stability		–	.005	.015	–	.005	.015	%/°C
Ref Short Ckt Current	V_{REF} = 0, T_A = 25°C	–	15	25	–	15	25	mA
Line Regulation	8V ≤ V_{IN} ≤ 40V	–	.005	.01	–	.005	.02	%/V
Line Regulation	8V ≤ V_{IN} ≤ 20V, I_O = 25 mA	–	.01	.02	–	.01	.03	%/V
Load Regulation	1 mA ≤ I_O ≤ 25 mA	–	.002	.004	–	.002	.004	%/mA
Load Regulation	1 mA ≤ I_O ≤ 100 mA	–	.002	.005	–	.002	.005	%/mA
Current Limit Sense Voltage	R_{SC} = 100Ω, V_O = 0	.06	.08	.10	.06	.08	.10	Volts
Shutdown Voltage Threshold		.40	.70	1.0	.40	.70	1.0	Volts
Shutdown Source Current	V_O = high	100	200	300	100	200	300	μA
Zener Voltage	J-Package only	6.0	6.4	7.0	6.0	6.4	7.0	Volts
Standby Current	V_{IN} = 40V	–	2.5	3.5	–	2.5	3.5	mA
Error Amplifier Offset Voltage		–	2.0	10	–	2.0	15	mV
Error Amplifier Input Bias Current		–	4	15	–	4	20	μA
Open Loop Gain	T_A = 25°C	66	68	72	60	68	72	dB
Ripple Rejection	f = 120Hz, T_A = 25°C	–	66	–	–	66	–	dB
Output Noise	10Hz ≤ f ≤ 100kHz, T_A = 25°C	–	50	–	–	50	–	μV_{rms}
Long Term Stability	V_{IN} = 30V, T_A = 125°C	–	0.3	1.0	–	0.3	1.0	%/kHr
Thermal Shutdown		–	175	–	–	175	–	°C

Note 1: Unless otherwise specified, V_{IN} = 10V, V_O = 5V, I_O = 1 mA, T_A = specified operating range.

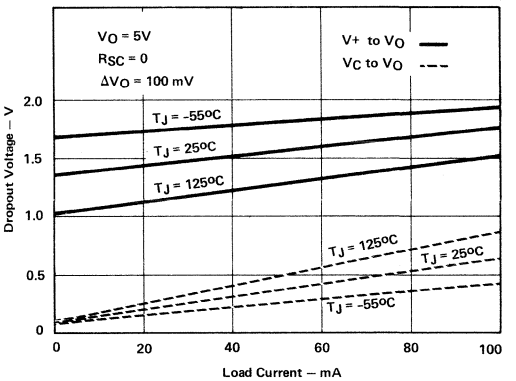
Note 2: All regulation specifications are measured at constant junction temperature using low duty-cycle pulse test.



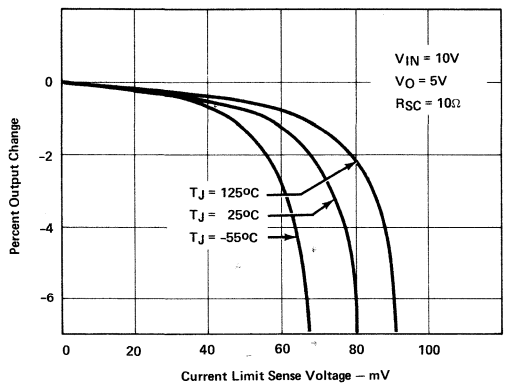
STANDBY CURRENT



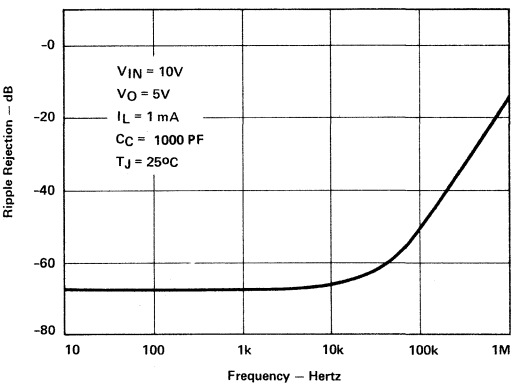
MINIMUM INPUT — OUTPUT VOLTAGE



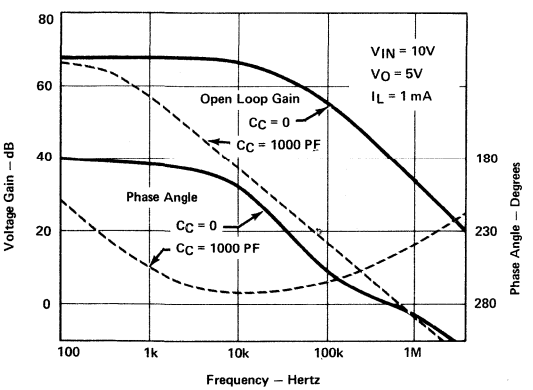
CURRENT LIMITING



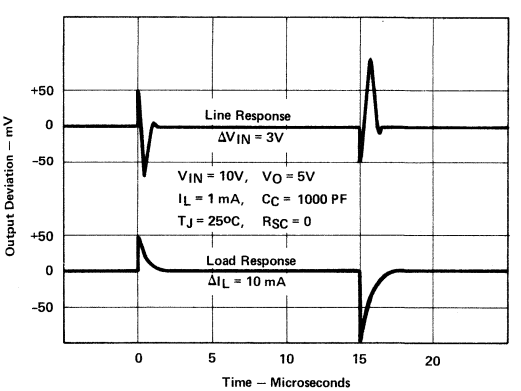
RIPPLE REJECTION



FREQUENCY RESPONSE



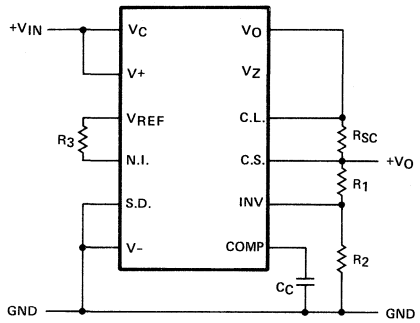
TRANSIENT RESPONSE



SG1532 / SG2532 / SG3532

APPLICATIONS

BASIC LOW CURRENT REGULATOR



$V_O = V_{REF}\left(1 + \frac{R_1}{R_2}\right)$

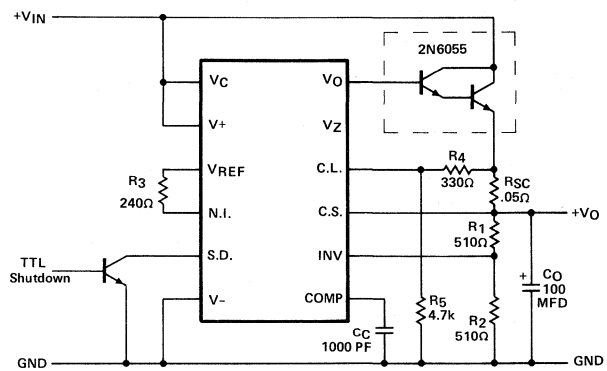
$R_3 = \frac{R_1 R_2}{R_1 + R_2}$

$I_{SC} = \frac{\text{Sense Voltage}}{R_{SC}}$

C_C = 1000 PF

I_O to 100 mA

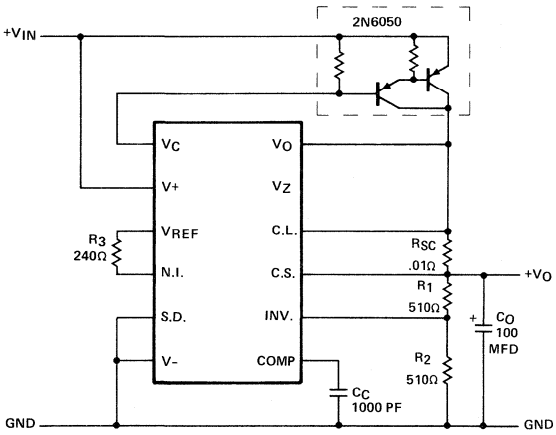
HIGH CURRENT REGULATOR WITH FOLDBACK CURRENT LIMITING AND REMOTE SHUTDOWN



Output Voltage = 5V
Max Output Current = 8A
Min V_{IN} at No Load = 6.9V
Min V_{IN} at 5A = 8.2V

Line Reg 10 - 30V = 3 mV
Load Reg 0 - 5A = 17 mV
Short Circuit Current = 1.8A

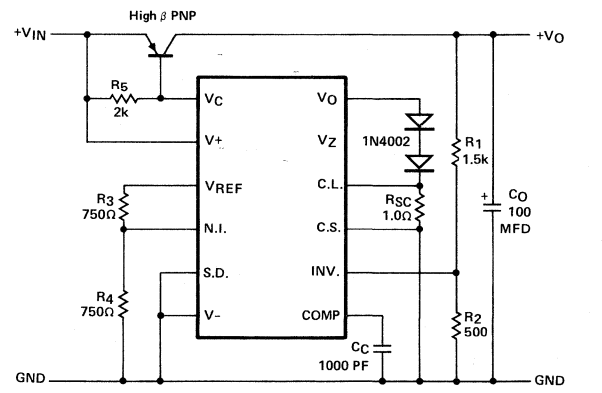
HIGH EFFICIENCY, LOW VOLTAGE REGULATOR



Output Voltage = 5V
Max Output Current = 9A
Min V_{IN} at 5A = 7.0V

Line Reg 7 - 20V = 10 mV
Load Reg 0 - 5A = 25 mV
Constant Current Limiting

90% EFFICIENT LINEAR REGULATOR



Output Voltage = 5V (Note 1)
Max Output Current = 3A (Note 2)
Min (V_{IN} - V_O) at 2A = 0.4V
Line Reg 6 - 30V = 10 mV
Load Reg 0 - 2A = 20 mV

Notes:

1. For output voltages above 8 volts and load currents which allow PNP base current to be limited to 25 mA, the internal zener may be used, eliminating the need for the two external diodes and the divider on V_{REF}.

2. R_{SC} can be eliminated if the 200 mA current limit on V_O is adequate. Overall current limiting is dependent upon PNP β. For greater accuracy, load current may be sensed in the ground line.

VOLTAGE SENSING CIRCUIT

SG1542 / SG2542 / SG3542

DESCRIPTION

This monolithic integrated circuit provides the control functions necessary to protect sensitive electronic circuitry from over-voltage transients or the effects of voltage regulator failure. It is designed for use with an external SCR "crowbar" for immediate shutdown of the power supply, but additionally provides logic level outputs for regulator turn-off and/or operator or system out-of-tolerance indication.

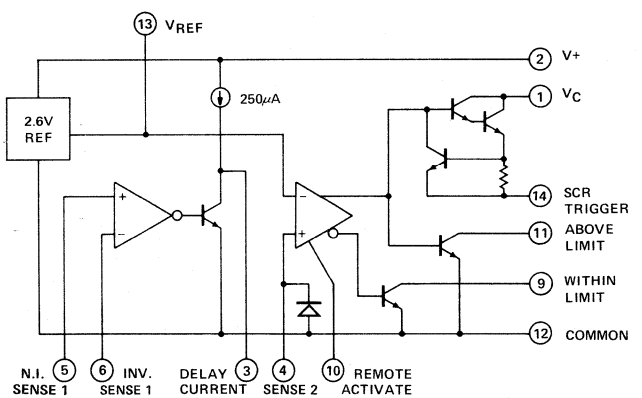
This device contains an accurate, stable 2.6 volt reference which allows the sensing threshold to be set predictably without the need for potentiometers. Uncommitted availability of both polarity inputs to the sensing comparator allows a wide flexibility of use including the ability to sense voltages less than the reference voltage. An external capacitor can be used to program an accurate time delay between fault occurrence and crowbar triggering, but this delay may be bypassed by inputing at the Sense 2 terminal or by using the remote activation capability.

For additional circuit functions, see SG1543 data sheet.

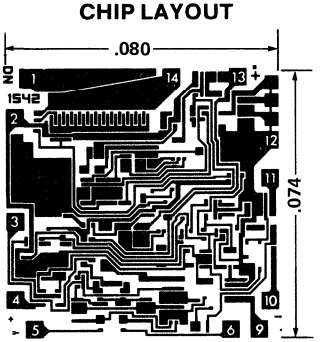
FEATURES

- **Operation from 4.5 to 40 volts**
- **Useful for either over- or under-voltage sensing**
- **Sensing threshold accurate to ±2%**
- **Built-in input hysteresis**
- **Zero to 35 volt sensing capability**
- **Programmable time delay**
- **SCR "Crowbar" drive of 200mA**
- **Remote activation capability**
- **2.6V 1% reference available**

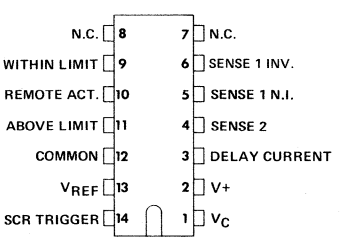
BLOCK DIAGRAM



CHIP LAYOUT



CONNECTION DIAGRAM



J, N PACKAGES (TO-116)

SG1542 / SG2542 / SG3542

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V+	40V
Collector Supply Voltage, V_C	40V
Sense Voltage (1)	V+
Sense Voltage (2)	6.5V
Remote Activation Input Voltage	7.0V
SCR Trigger Current	300mA*
Limit Indicators Output Voltage	40V
Limit Indicators Output Sink Current	50mA

Power Dissipation (Package Limitation)	1000mW
Derate above 25° C	8.0 mW/° C
Operating Temperature Range	
SG1542	−55° C to +125° C
SG2542	−25° C to +85° C
SG3542	0° C to +70° C
Storage Temperature Range	−65° C to +150° C

*At higher input voltages, a dissipation limiting resistor, R_G, is required. See graph.

ELECTRICAL CHARACTERISTICS

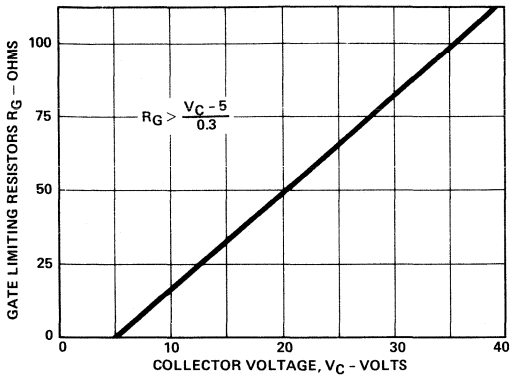
(Unless otherwise stated, these specifications apply for V+ = 5 to 35V and T_J = −55° C to +125° C for the SG1542, −25° C to +85° C for the SG2542, and 0° C to +70° C for the SG3542.)

PARAMETER	CONDITIONS	SG1542/2542			SG3542			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range	T_J = 25°C to T_{max}	4.5	—	40	4.5	—	40	V
Input Voltage Range	T_{min} to T_{max}	4.7	—	40	4.7	—	40	V
Supply Current	V+ = 40V, Outputs open	—	5	7	—	5	10	mA
Reference Voltage	T_J = 25°C	2.58	2.60	2.62	2.55	2.60	2.65	V
Reference Voltage	Over Temp. Range	2.55	—	2.65	2.50	—	2.70	V
Line Regulation	V+ = 5 to 40V	—	1	5	—	1	5	mV
Load Regulation	I_{REF} = 0 to 10mA	—	1	10	—	1	10	mV
Short Circuit Current	V_{REF} = 0	12	15	25	12	15	25	mA
Temperature Stability		—	.005	—	—	.005	—	%/°C
Sense 1 Offset Voltage	Sense 1 (+) rising	-10	0	+10	-20	0	+20	mV
Sense 1 Offset Voltage	Sense 1 (+) falling	-35	-25	-15	-50	-25	0	mV
Sense 1 Common Mode		0	—	(V+) −3	0	—	(V+) −3	V
Sense 1 Bias Current		—	-0.3	-1.0	—	-0.3	-1.0	μA
Sense 2 Threshold		2.50	2.60	2.70	2.50	2.60	2.70	V
Sense 2 Bias Current		—	1.0	10	—	1.0	10	μA
Delay Current		200	250	300	200	250	300	μA
Remote Activation Current		—	120	180	—	120	180	μA
Remote Act. Threshold		0.8	1.0	2.0	0.8	1.0	2.0	V
Peak Output Current	V_C = 5V, R_G = 0, V_O = 0	100	200	400	100	200	400	mA
Peak Output Voltage	I_O = 100mA	V_{IN} −2	V_{IN} −1.6	—	V_{IN} −2	V_{IN} −1.6	—	V
Output Off Voltage	V+ = V_C = 40V	—	0	0.1	—	0	0.1	V
Limit Indicators V_{SAT}	I_L = -10mA	—	0.2	0.5	—	0.2	0.5	V
Limit Indicators Leakage	V_{IND} = 40V	—	.01	1.0	—	.01	1.0	μA
Propagation Delay	T_O Ind., T_J = 25°C	—	500	—	—	500	—	nS
Propagation Delay	T_O Trigger, T_J = 25°C	—	500	—	—	500	—	nS
Output Current Rise Time	R_L = 50Ω, T_J = 25°C	—	400	—	—	400	—	mA/μS

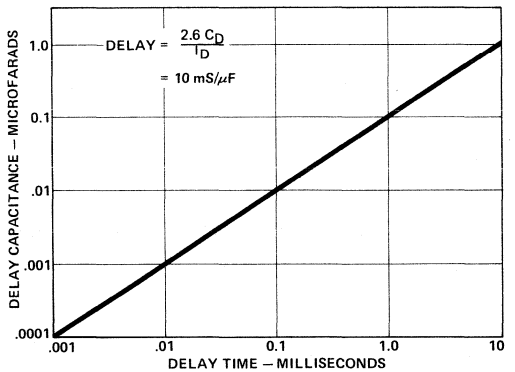
SG1542 / SG2542 / SG3542

TYPICAL CHARACTERISTICS

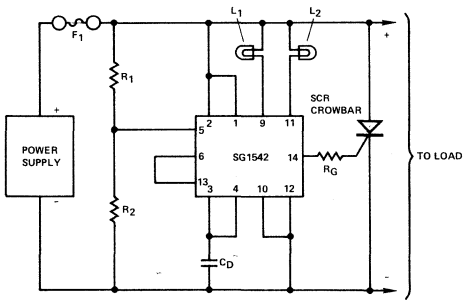
MINIMUM GATE CURRENT LIMITING RESISTANCE



ACTIVATION DELAY VS. CAPACITOR VALUE



BASIC OVER-VOLTAGE PROTECTION CIRCUIT CONFIGURATION



F_1 = Only necessary if power supply is not current limited

$V_{TRIP} = \left[\frac{2.6V\ (R_1 + R_2)}{R_2}\right]$, $R_2 \leqslant 100k\Omega$

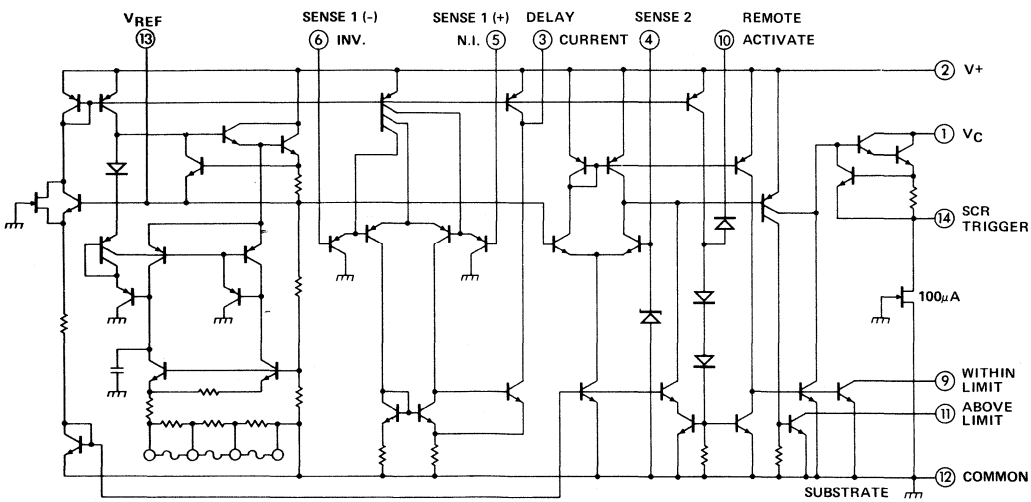
$t_D = 10^4\ C_D$

$R_G > \frac{V_C - 5}{0.3}$

L_1, L_2 = Indicator selected for max. current ≈ 10mA @ V_{TRIP}

SCR = Selected for max. peak current capability

SG1542 SIMPLIFIED SCHEMATIC DIAGRAM

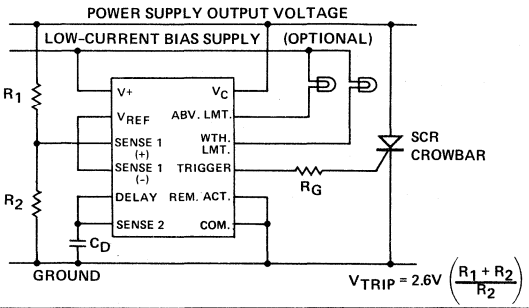


VOLTAGE SENSING CIRCUIT

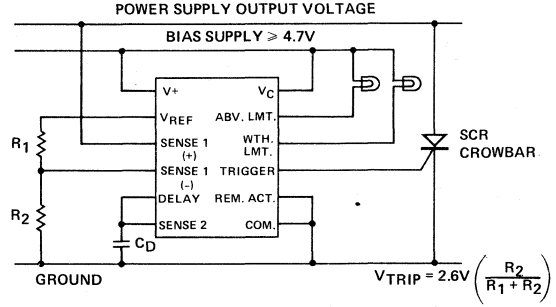
SG1542 / SG2542 / SG3542

APPLICATIONS

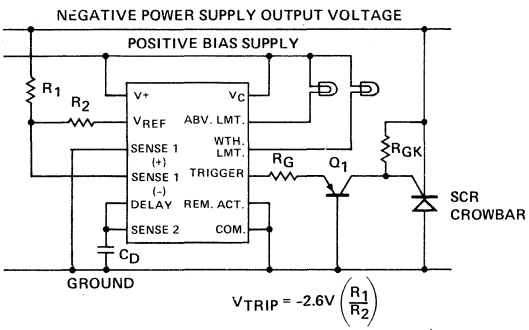
OVER-VOLTAGE SENSING FOR VOLTAGES ABOVE 2.6 VOLTS



OVER-VOLTAGE SENSING FOR VOLTAGES LESS THAN 2.6 VOLTS

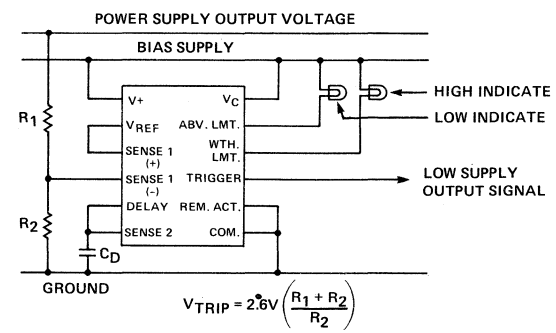


OVER-VOLTAGE SENSING FOR NEGATIVE OUTPUT VOLTAGES*

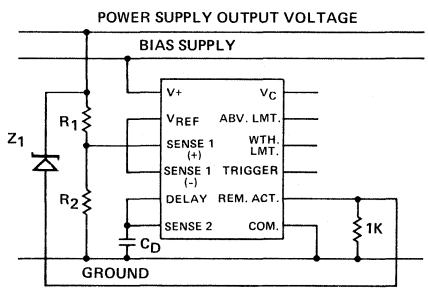


*Without a positive bias supply, the basic OVP circuit on page 3 can be used equally well with either positive or negative voltages.

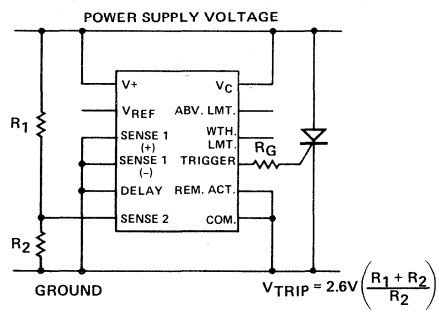
UNDER-VOLTAGE SENSING



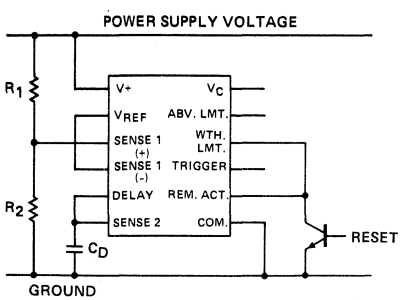
DELAYED THRESHOLD SENSE PLUS IMMEDIATE TRIP FOR HIGH OVER-VOLTAGE



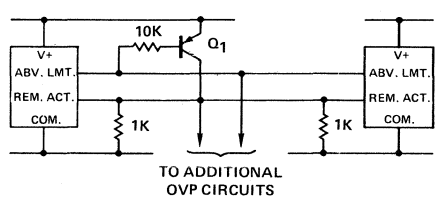
OVER-VOLTAGE SENSING WITH MINIMUM TIME DELAY



OVER-VOLTAGE LATCH WITH RESET



INTERCONNECTING MULTIPLE SG1542'S



Q1 must provide >2mA for each OVP circuit. With this arrangement, activation of any circuit will activate all. For a master-slave relationship, the WITHIN LIMIT terminal of the master may be directly connected to the REMOTE ACTIVATE terminals of all the slaves.

Power Supply Output Supervisory Circuit

SG1543 / 2543 / 3543

DESCRIPTION

This monolithic integrated circuit contains all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR "crowbar" shutdown; an under-voltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage; and a third op amp/comparator usable for current sensing (C.L.) are all included in this IC, together with an independent, accurate reference generator.

Both over and under-voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-or'ed together, and although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs, or from an external signal. The O.V. circuit also includes an optional latch and external reset capability.

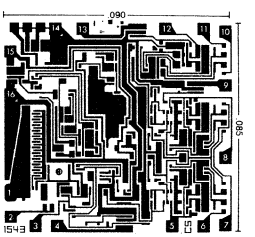
The current sense circuit may be used with external compensation as a linear amplifier or as a high-gain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

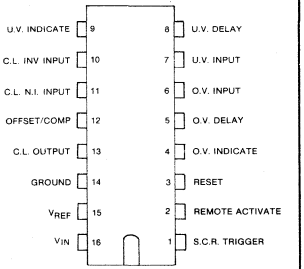
FEATURES

- **Over-voltage, under-voltage, and current sensing circuits all included**
- **Reference voltage trimmed to 1% accuracy**
- **SCR "Crowbar" drive of 300 mA**
- **Programmable time delays**
- **Open-collector outputs and remote activation capability**
- **Total standby current less than 10mA**

CHIP LAYOUT



CONNECTION DIAGRAM



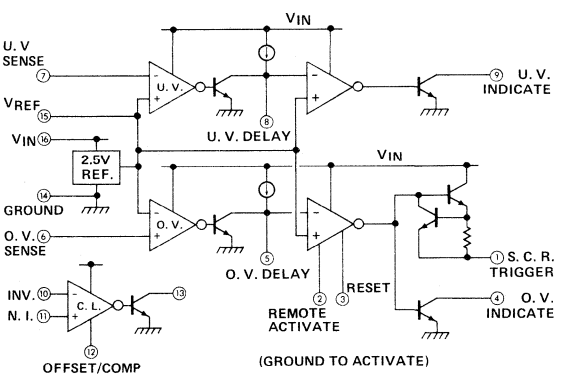
J-Package
TO-116 Cerdip

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN}	40V
Sense Inputs	V_{IN}
SCR Trigger Current	300mA*
Indicator Output Voltage	40V
Indicator Output Sink Current	50mA
Power Dissipation (Package Limitation)	1000mW
Derate Above 25° C	8.0mW/° C
Operating Temperature Range	
SG1543	−55° C to +125° C
SG2543	−25° C to +85° C
SG3543	0° C to +70° C
Storage Temperature Range	−65° C to +150° C

* At higher input voltages, a dissipation limiting resistor, R_G, is required.

BLOCK DIAGRAM



SG1543 / 2543 / 3543

ELECTRICAL CHARACTERISTICS

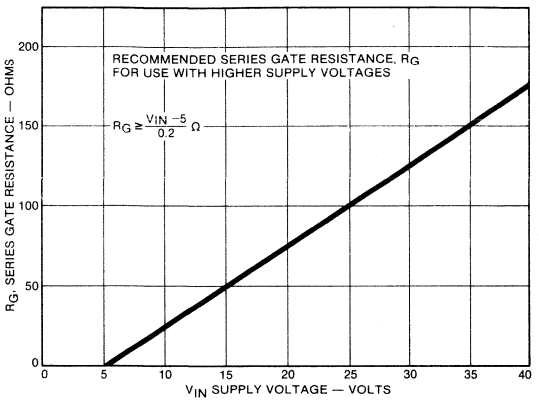
(Unless otherwise stated, these specifications apply for T_J = −55° C to +125° C for the SG1543, −25° C to +85° C for the SG2543 and 0° C to +70° C for the SG3543; and for V_{IN} = 10 Volts.

PARAMETER	CONDITIONS	SG1543/2543			SG3543			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range	T_J = 25°C to T_{max}	4.5	–	40	4.5	–	40	V
Input Voltage Range	T_{min} to T_{max}	4.7	–	40	4.7	–	40	V
Supply Current	T_J = 25°C, V_{IN} = 40V	–	7	10	–	7	10	mA
REFERENCE SECTION (Pins 15, 16)								
Output Voltage	T_J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
Output Voltage	Over Temp. Range	2.45	–	2.55	2.40	–	2.60	V
Line Regulation	V_{IN} = 5 to 30V	–	1	5	–	1	5	mV
Load Regulation	I_{REF} = 0 to 10 mA	–	1	10	–	1	10	mV
Short Circuit Current	V_{REF} = 0	12	15	25	12	15	25	mA
Temperature Stability		–	50	–	–	50	–	ppm/°C
SCR TRIGGER SECTION (Pins 1, 2, 3)								
Peak Output Current	V_{IN} = 5V, R_G = 0, V_O = 0	100	200	400	100	200	400	mA
Peak Output Voltage	V_{IN} = 15V, I_O = 100mA	12	13	–	12	13	–	V
Output Off Voltage	V_{IN} = 40V	–	0	0.1	–	0	0.1	V
Remote Activate Current	Pin 2 = Gnd	–	.4	.8	–	.4	.8	mA
Remote Activate Voltage	Pin 2 open	–	2	6	–	2	6	V
Reset Current	Pin 3 = Gnd, Pin 2 = Gnd	–	.4	.8	–	.4	.8	mA
Reset Voltage	Pin 3 open, Pin 2 = Gnd	–	2	6	–	2	6	V
Output Current Rise Time	R_L = 50Ω	–	400	–	–	400	–	mA/μS
Prop. Delay from Pin 2	T_J = 25°C, $V_{(Pin\ 2)}$ = 0.4V	–	300	–	–	300	–	nS
Prop. Delay from Pin 6	C_D = 0, $V_{(Pin\ 6)}$ = 2.7V,	–	500	–	–	500	–	nS
COMPARATOR SECTIONS (Pins 6, 7, 5, 8, 4, 9)								
Input Threshold (Input voltage rising on Pin 6 and falling on Pin 7)	T_J = 25°C	2.45	2.50	2.55	2.40	2.50	2.60	V
	Over Temp. Range	2.40	–	2.60	2.35	–	2.65	V
Input Hysteresis		–	25	–	–	25	–	mV
Input Bias Current	Sense input = 0V	–	0.3	1.0	–	0.3	1.0	μA
Delay Saturation		–	0.2	0.5	–	0.2	0.5	V
Delay High Level		–	6	7	–	6	7	V
Delay Charging Current	V_D = 0V	200	250	300	200	250	300	μA
Indicate Saturation	I_L = -10mA	–	0.2	0.5	–	0.2	0.5	V
Indicate Leakage	V_{IND} = 40V	–	.01	1.0	–	.01	1.0	μA
Propagation Delay	$V_{(Pin\ 6)}$ = 2.7V, $V_{(Pin\ 7)}$ = 2.3V, T_J = 25°C; C_D = 0	–	400	–	–	400	–	nS
	C_D = 1μf	–	10	–	–	10	–	mS
CURRENT LIMIT SECTION (Pins 10, 11, 12, 13)								
Input Voltage Range		0	–	(V_{IN} −3V)	0	–	(V_{IN} −3V)	V
Input Bias Current	Pin 12 open, V_{CM} = 0V	–	0.3	1.0	–	0.3	1.0	μA
Input Offset Voltage	Pin 12 open, V_{CM} = 0V	–	0	10	–	0	15	mV
Input Offset Voltage	10kΩ from Pin 12 to Gnd	80	100	120	70	100	130	mV
CMRR	0 ≤ V_{CM} ≤ 12V, V_{IN} = 15V	60	70	–	60	70	–	dB
AVOL	Pin 12 open, V_{CM} = 0V	72	80	–	72	80	–	dB
Output Saturation	I_L = -10mA	–	0.2	0.5	–	0.2	0.5	V
Output Leakage	V_{IND} = 40V	–	.01	1.0	–	.01	1.0	μA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C	–	5	–	–	5	–	MHz
Propagation Delay	$V_{overdrive}$ = 100mV, T_J = 25°C	–	200	–	–	200	–	nS

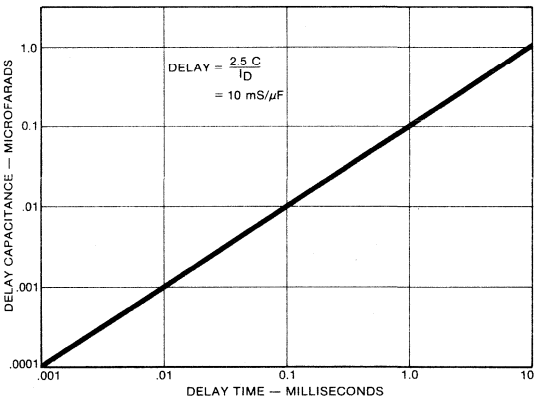
SG1543 / 2543 / 3543

TYPICAL CHARACTERISTICS

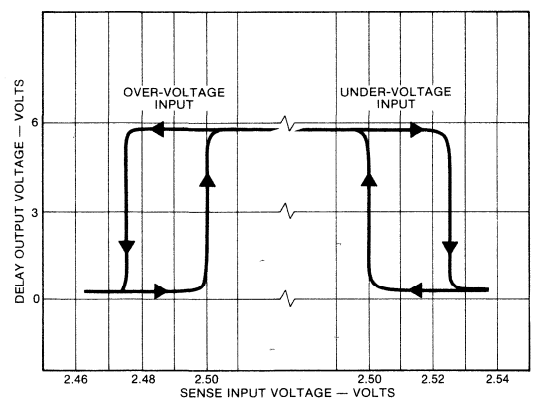
SCR TRIGGER POWER LIMITING



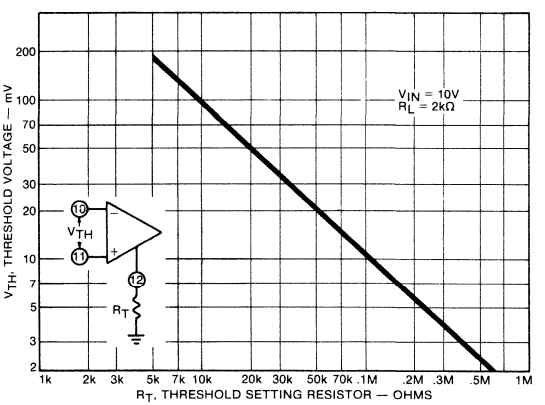
ACTIVATION DELAY VS. CAPACITOR VALUE



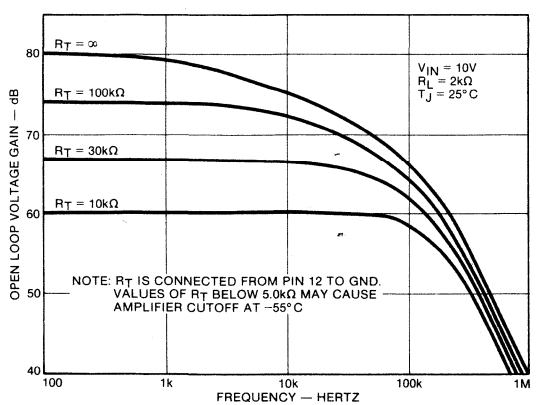
COMPARATOR INPUT HYSTERESIS



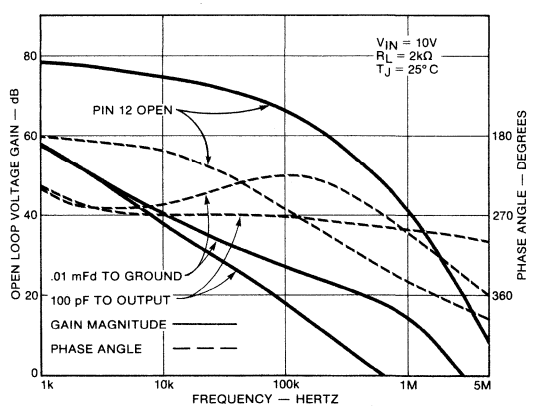
CURRENT LIMIT INPUT THRESHOLD



CURRENT LIMIT AMPLIFIER GAIN



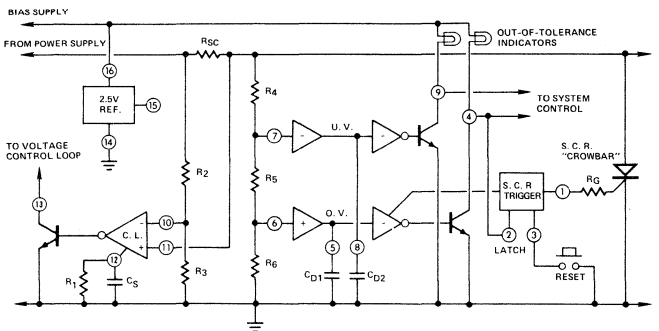
CURRENT LIMIT AMPLIFIER FREQUENCY RESPONSE



SG1543 / 2543 / 3543

APPLICATIONS

TYPICAL APPLICATION



The values for the external components are determined as follows:

Current limit input threshold, $Vth \approx \frac{1000}{R1}$

Cs is determined by the current loop dynamics

Peak current to load, $Ip \cong \frac{Vth}{Rsc} + \frac{Vo}{Rsc}\left(\frac{R2}{R2 + R3}\right)$

Short circuit current, $Isc = \frac{Vth}{Rsc}$

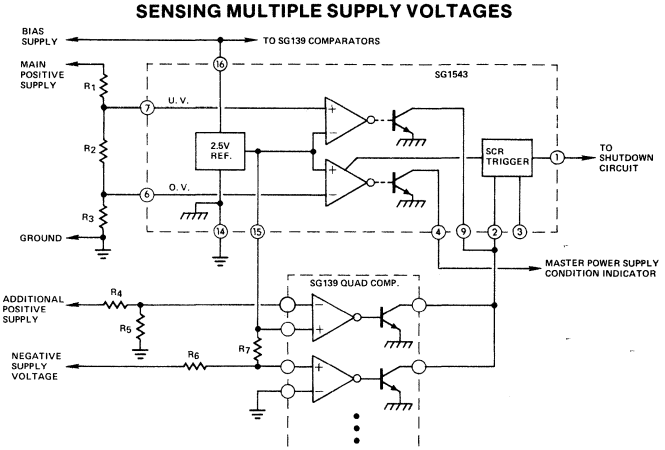
Low output voltage limit, $Vo\ (Low) = \frac{2.5\ (R4 + R5 + R6)}{R5 + R6}$

High output voltage limit, $Vo\ (High) = \frac{2.5\ (R4 + R5 + R6)}{R6}$

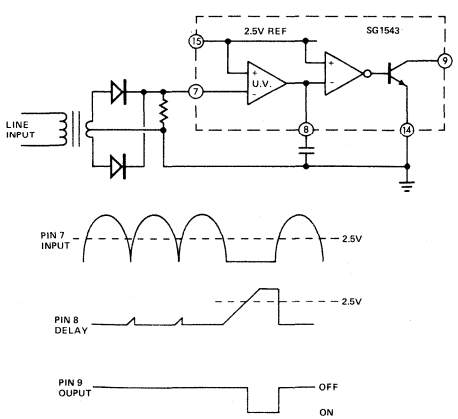
Voltage sensing delay, td = 10,000 Cd

SCR trigger power limiting resistor, $Rg > \frac{Vin - 5}{0.2}$

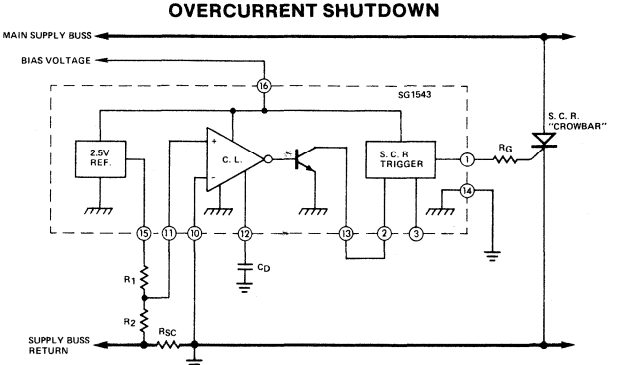
SENSING MULTIPLE SUPPLY VOLTAGES



INPUT LINE MONITOR



OVERCURRENT SHUTDOWN



Data subject to change without notice.

SG1568/1468

SG1568/1468 is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100mA. The device is set internally for ±15V outputs but a single external adjustment can be used to change both outputs simultaneously from 14.5 to 20 volts. Input voltages up to ±30 volts can be used and there is provision for adjustable current limiting.

- **Outputs balanced to within 1% (SG1568)**
- **Line and load regulation of 0.06%**
- **1% maximum output variation due to temperature changes**
- **Standby current drain of 3.0mA**
- **Remote sensing provisions**

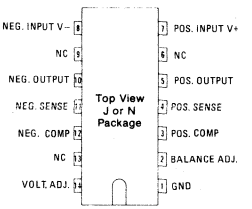
PARAMETERS*	SG1568	SG1468	UNIT
Operating Temperature Range	−55 to +125	0 to +75	°C
Package Types	T, J	T, J, N	—
Peak Load Current	100		mA
Storage Junction Temp Range	−65 to +175		°C
Output Voltage	14.8/15.2	14.5/15.5	V
Input Voltage	30	30	V
Input-Output Voltage Differential	2.0	2.0	V
Output Voltage Balance	±150	±300	mV
Line Regulation Voltage			
(V_{in} = 18V to 30V)	10	10	mV
(T_{low}[1] to T_{high}[2])	20	20	
Load Regulation Voltage			
(I_L = 0 to 50 mA, T_J = constant)	10	10	mV
(T_A = T_{low} to T_{high})	30	30	
Output Voltage Range	8/20	8/20	V
Ripple Rejection (f = 120Hz)	75 (typ)	75 (typ)	dB
Output Voltage Temperature Stability			
(T_{low} to T_{high})	1.0	1.0	%
Short-Circuit Current Limit			
(R_{SC} = 10 ohms)	60 (typ)	60 (typ)	mA
Output Noise Voltage			
(BW = 100Hz − 10kHz)	100 (typ)	100 (typ)	μV(rms)
Positive Standby Current			
(V_{in} = +30V)	4.0	4.0	mA
Negative Standby Current			
(V_{in} = −30V)	3.0	3.0	mA
Long-Term Stability	0.2 (typ)	0.2 (typ)	%/k Hr

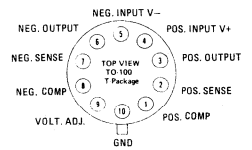
(VCC = +20V, V_{EE} = −20V, C1 = C2 = 1500 pF, C3 = C4 = 1.0 μF, $R_{SC}^+ = R_{SC}^- = 4.0\Omega$, $I_L^+ = I_L^- = 0$, T_C = +25°C unless otherwise noted.)

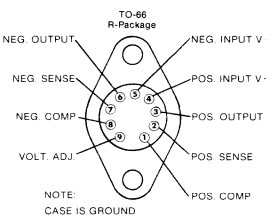
[1] T_{low} = 0°C for 1468
= −55°C for 1568

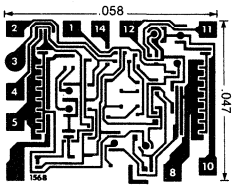
[2] T_{high} = +75°C for 1468
= +125°C for 1568

CONNECTION DIAGRAMS



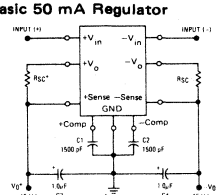






SG1568/1468 Chip (See J-Package diagram for pad functions)

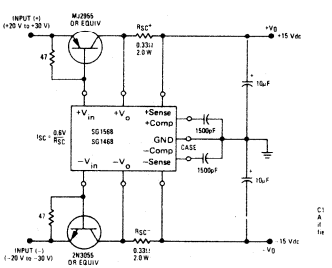
Basic 50 mA Regulator



C1 and C2 should be located as close to the device as possible. A 0.1μF ceramic capacitor may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors.

C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation it may be necessary to bypass C4 with a 0.1μF ceramic disc capacitor.

±1.5 Amp Regulator (Short Circuit Protected, with Proper Heatsinking)



See Applications Notes for additional information.

SG3523 / 3523A / 3423 / 3423A

DESCRIPTION

This monolithic integrated circuit provides the control functions necessary to protect sensitive electronic circuitry from over-voltage transients or the effects of voltage regulator failure. It is designed for use with an external SCR "crowbar" for immediate shutdown of the power supply, but additionally provides logic level outputs for regulator turn-off and/or operator or system out-of-tolerance indication.

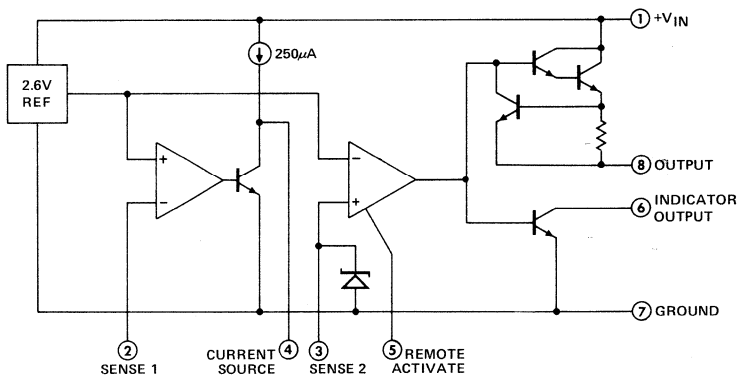
This device contains an accurate, stable 2.6 volt reference which allows the sensing threshold to be set predictably without the need for potentiometers. An external capacitor can be used to program an accurate time delay between fault occurence and crowbar triggering, but this delay may be bypassed by inputing at the Sense 2 terminal or by using the remote activation capability.

For additional circuit functions, see SG1542 and SG1543 data sheets.

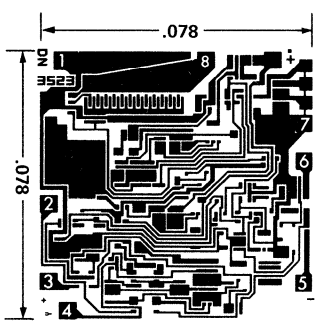
FEATURES

- **Operation from 4.5 to 40 volts**
- **Highly accurate sensing threshold**
- **Built-in input hysteresis**
- **Programmable time delay**
- **SCR "Crowbar" drive of 200mA**
- **Remote activation capability**

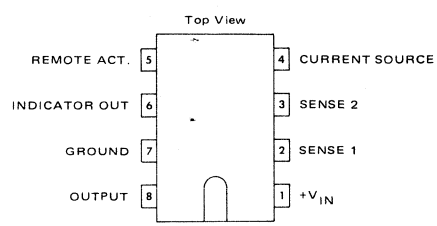
BLOCK DIAGRAM



CHIP LAYOUT



CONNECTION DIAGRAM



Y, M-PACKAGES (MINIDIP)

SG3523 / 3523A / 3423 / 3423A

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN}	40V
Sense Voltage (1)	V_{IN}
Sense Voltage (2)	6.5V
Remote Activation Input Voltage	7.0V
SCR Trigger Current	300mA
Indicator Output Voltage	40V
Indicator Output Sink Current	50mA

Power Dissipation (Package Limitation)	
Ceramic minidip (Y-pkg.)	800mW
Derate above 25° C	8.0mW/° C
Plastic minidip (M-pkg.)	400mW
Derate above 25° C	4.0 mW/° C
Operating Temperature Range	
SG3523/3523A	−55° C to +125° C
SG3423/3423A	0° C to +70° C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply for V_{IN} = 5 to 35V and T_J = −55° C to +125° C for the SG3523/3523A and 0° C to +70° C for the SG3423/3423A.)

PARAMETER	CONDITIONS	SG3523A			SG3423A			SG3423/SG3523			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Range		4.5	–	40	4.5	–	40	4.5	–	40	V
Supply Current		–	5	7	–	5	7	–	5	10	mA
Sense Threshold	T_J = 25°C	2.55	2.60	2.65	2.50	2.60	2.70	2.45	2.60	2.75	V
Sense Threshold	Over Temp. Range	2.50	–	2.70	2.45	–	2.75	2.35	–	2.85	V
Input Hysteresis	Sense 1 only	–	25	–	–	25	–	–	25	–	mV
Input Bias Current	Sense 1	–	-0.3	-1.0	–	-0.3	-1.0	–	–	–	μA
	Sense 2	–	+5	+10	–	+5	+10	–	–	–	μA
Current Source		200	250	300	200	250	300	100	250	300	μA
Remote Activation Input Current	$V_{Pin\ 5}$ = 2.0	–	5	40	–	5	40	–	5	40	μA
	$V_{Pin\ 5}$ = 0.8V	–	-120	-180	–	-120	-180	–	-120	-180	μA
Output Voltage	I_O = 100mA	V_{IN} −2.2	V_{IN} −1.8	–	V_{IN} −2.2	V_{IN} −1.8	–	V_{IN} −2.2	V_{IN} −1.8	–	V
Peak Output Current	V_{IN} = 5V, V_O = 0V	–	200	300	–	200	300	–	–	–	mA
Output Off Voltage	V_{IN} = 40V	–	0	0.1	–	0	0.1	–	–	–	V
Indicator Saturation Voltage	I_L = -1.6mA	–	0.1	–	–	0.1	–	–	0.1	0.4	V
	I_L = -10mA	–	0.2	0.5	–	0.2	0.5	–	0.4	–	V
Indicator Leakage	$V_{Pin\ 6}$ = 40V	–	.01	1.0	–	.01	1.0	–	–	–	μA
Propagation Delay to Output	T_J = 25°C, Sense 1	–	1.0	–	–	1.0	–	–	1.0	–	μS
	T_J = 25°C, Sense 2	–	0.5	–	–	0.5	–	–	0.5	–	μS
Output Current Rise Time	T_J = 25°C	–	400	–	–	400	–	–	400	–	mA/μS

SILICON GENERAL
11651 Monarch Street • Garden Grove, CA 92641 • (714) 892-5531 • TWX: 910-596-1804 • Telex: 69-2411

SG4194

DESCRIPTION

The SG4194 is a dual polarity tracking regulator designed to provide balanced or unbalanced output voltages at currents up to 200 mA. Both output voltages may be programmed between the limits of ±100 mV and ±42 volts by a single resistor. A balance terminal allows adjustment for non-symmetrical positive and negative output voltages.

This device is designed for ease of application with a minimal number of external components. In addition, internal current limiting and thermal shutdown provide full overload protection.

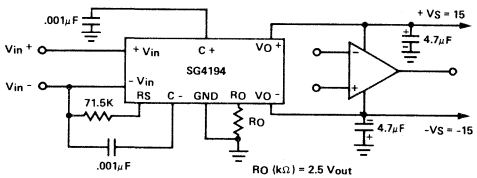
The SG4194 regulator is available in two package types to meet a wide range of dissipation requirements. The R (TO-66) power package is rated at 3W at T_A = 25°C, while the J (TO-116) 14-pin ceramic DIP will dissipate 1W at T_A = 25°C.

- **Simultaneously adjustable outputs with one resistor to ±42V**
- **Load current ±200mA**
- **Internal thermal shutdown at T = 175° C**
- **Provision for ±V unbalancing**
- **3W power dissipation**
- **.2% load regulation**

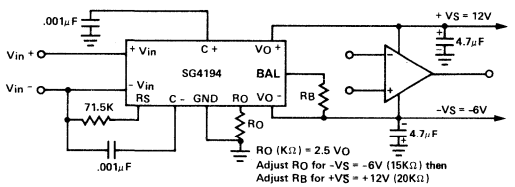
ABSOLUTE MAXIMUM RATINGS

Input Voltage ±V to Ground . . . . . SG4194: ±45V
SG4194C: ±35V
Input-Output Voltage Differential . . . . . SG4194: ±45V
SG4194C: ±35V
Power Dissipation at T_A = 25°C
J Package 1.0W
Derate above 25°C . . . . . 8 mW/°C
R Package 3.0W
Derate above 25°C . . . . . 24 mW/°C
Load Current
J Package . . . . . 150 mA
R Package . . . . . 250 mA
Operation Junction Temperature Range
SG4194 . . . . . -55°C to +150°C
SG4194C . . . . . 0°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . . +300°C

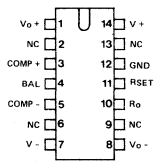
Balanced Output Voltage —



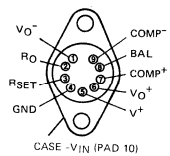
Unbalanced Output Voltage —



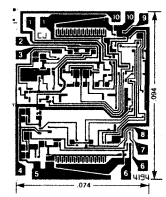
CONNECTION DIAGRAMS



"J" Dual In-Line Package
(TOP VIEW)
SG4194 J
SG4194CJ



"R" (TO-66) Package
(TOP VIEW)
SG4194 R
SG4194CR



R-Package
Pin Numbers

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	SG4194			SG4194C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	ΔV_{in} = 0.1V_{in}		0.02	0.1		0.02	0.1	% V_{out}
Load Regulation	4194R: I_L = 1 to 200 mA 4194J: I_L = 1 to 100 mA		0.001	0.002		0.001	0.004	% V_O/mA
TC of Output Voltage			0.002	0.015		0.003	0.015	%/°C
Stand-By Current Drain (Note 1)	V_{in} = V_{max}, V_O = 0V		+0.3	+1.0		+0.3	+1.5	mA
	V_{in} = V_{max}, V_O = 0V		-1.2	-2.0		-1.2	-3.0	
Input Voltage Range		±9.5		±45	±9.5		±35	V
Output Voltage Scale Factor	R_{set} = 71.5K, T_j = 25°C	2.45	2.5	2.55	2.38	2.5	2.62	KΩ/V
Output Voltage Range	R_{set} = 71.5K	0.10		±42	0.10		±32	V
Output Voltage Tracking				1.0			2.0	%
Ripple Rejection	f = 120Hz, T_j = 25°C		70			70		dB
Input-Output Voltage Differential	I_L = 50mA	3.0			3.0			V
Output Short Circuit Current	V_{in} = ±30V Max		300			300		mA
Output Noise Voltage	C_L = 4.7μF, V_O = ±15V f = 10Hz to 100kHz		250			250		μV RMS
Internal Thermal Shutdown			175			175		°C

Note 1: ±$I_{Quiescent}$ will increase by 50μA/V_{out} on positive side and 100μA/V_{out} on negative side.

SG7800 / 7800C
SG140 / 240 / 340
SG7800A / 7800AC

DESCRIPTION

The SG7800A/7800/140/240/340 series of positive regulators offer self contained, fixed-voltage capability with up to 1.5 amps of load current and input voltages up to 50 volts on the SG7800A series only.

These units feature a unique on-chip trimming system to set the output voltages to within ±1.5% of nominal on the SG7800A series, ±2.0% on the SG140/220 series, and ±4.0% on the SG7800/340 series. The SG7800A versions also offer much improved line and load regulation characteristics.

All protective features of thermal shutdown, current limiting, and safe-area control have been designed into these units and since these regulators require only a single output capacitor for satisfactory performance, ease of application is assured.

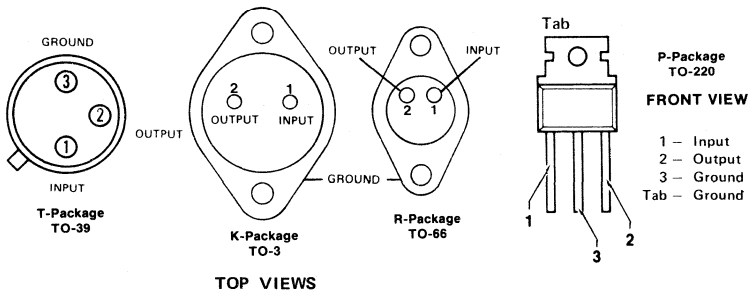
Although designed as fixed-voltage regulators, the output voltage can be increased through the use of a simple voltage divider. The low quiescent drain current of the device insures good regulation when this method is used.

Product is available in hermetically sealed TO-3, TO-39 and TO-66 power packages and commercial product is also available in the plastic TO-220 package.

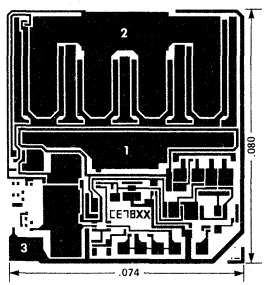
FEATURES

- **Output voltage set internally to ±1.5% on SG7800A**
- **Input voltage range to 50 volts max. on SG7800A**
- **Two volt input-output differential**
- **Excellent line and load regulation**
- **Foldback current limiting**
- **Thermal overload protection**
- **Voltages available — 5V, 6V, 8V, 12V, 15V, 18V, 20V, 24V**

CONNECTION DIAGRAMS



CHIP LAYOUT



ABSOLUTE MAXIMUM RATINGS

Device Output Voltage	Input Voltage	7800A Series Input Voltage	Input-Output Differential
5V	35V	50V	35V
6V	35V	50V	35V
8V	35V	50V	35V
12V	35V	50V	35V
15V	35V	50V	35V
18V	35V	50V	35V
20V	35V	50V	35V
24V	40V	50V	35V

Operating Junction Temperature Range

SG7800A/7800/140 ..... −55° C to +150° C
SG240 ..... 0° C to +150° C
SG7800AC/7800C/340 ..... 0° C to +125° C

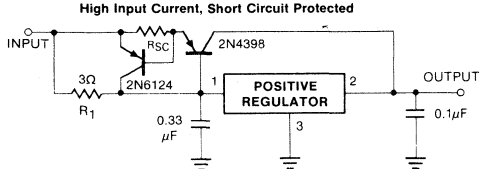
Storage Temperature Range ..... −65° C to +150° C
Lead Temperature (Soldering, 10 Sec) ..... +300° C

Power/Thermal Characteristics

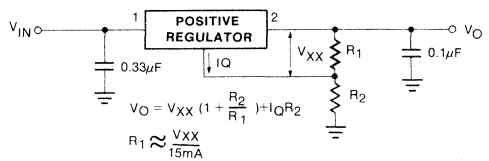
Package	K (TO-3)	R (TO-66)	P (TO-220)	T (TO-39)
25° C Case Rated Power	20W	15W	15W	2W
25° C Ambient Rated Power	4.3W	3.0W	2.0W	1.0W
Design Current	1.5A	1.5A	1.0A	0.5A
Therm. Res. θJC (°C/W)	3.0	5.0	3.0	15
θJA (°C/W)	35	40	60	120

APPLICATIONS

High Input Current, Short Circuit Protected



Circuit for Increasing Output Voltage



DEVICE PART NUMBERS			SG7805A			SG140-05			SG7805(109)			SG7805AC			SG340-05(309)			SG7805C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	4.92		5.08	4.8		5.2	4.8		5.2	4.92		5.08	4.8		5.2	4.8		5.2	V
Line Regulation		T_J = 25°C, V_{IN} = 7 to 25V		5	25		5	50		5	50		5	50		5	50		10	100	mV
		V_{IN} = 8 to 12V		2	12		2	25		2	25		2	25		2	25		4	50	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		15	50		15	50		15	50		15	50		15	50		25	100	mV
		I_O = 250 to 750mA		5	25		5	25		5	25		5	25		5	25		10	50	mV
	T-Pkg	I_O = 5mA to 500mA		5	25		5	25		5	25		5	25		5	25		20	100	mV
Total Output Voltage Tolerance V_{IN} = 8 to 20V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	4.85		5.15	4.75		5.25	4.65		5.35	4.85		5.15	4.75		5.25	4.75		5.25	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 8 to 25V			0.8			0.8			0.8			1.0			1.0			1.3	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2			2			2			2			2			2		V
		T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.5			2.5			2.5			2.5			2.5			2.5		A
		T-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		2.1			2.1			2.1			2.1			2.1			2.1		A
		T-Pkg		0.7			0.7			0.7			0.7			0.7			0.7		A
Temperature Coefficient		I_O = 5mA		−0.5			−0.5			−0.5			−0.5			−0.5			−0.5		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		78			78			78			78			78			78		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		40			40			40			40			40			40		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		20			20			20			20			20			20		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 10V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7806A			SG140-06			SG7806			SG7806A			SG340-06			SG7806C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	5.9		6.1	5.75		6.25	5.75		6.25	5.9		6.1	5.75		6.25	5.75		6.25	V
Line Regulation		T_J = 25°C, V_{IN} = 8 to 25V		6	30		6	60		6	60		6	60		6	60		12	120	mV
		V_{IN} = 9 to 13V		3	15		3	30		3	30		3	30		3	30		6	60	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		20	60		20	60		20	60		20	60		20	60		40	120	mV
		I_O = 250 to 750mA		6	30		6	30		6	30		6	30		6	30		12	60	mV
	T-Pkg[1]	I_O = 5mA to 500mA		6	30		6	30		6	30		6	30		6	30		12	60	mV
Total Output Voltage Tolerance V_{IN} = 9 to 21V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	5.82		6.18	5.7		6.3	5.65		6.35	5.82		6.18	5.7		6.3	5.7		6.3	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 8 to 25V			0.8			0.8			0.8			1.0			1.0			1.3	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2			2			2			2			2			2		V
		T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.5			2.5			2.5			2.5			2.5			2.5		A
		T-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		2.0			2.0			2.0			2.0			2.0			2.0		A
		T-Pkg		0.6			0.6			0.6			0.6			0.6			0.6		A
Temperature Coefficient		I_O = 5mA		−0.5			−0.5			−0.5			−0.5			−0.5			−0.5		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		75			75			75			75			75			75		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		45			45			45			45			45			45		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		24			24			24			24			24			24		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 11V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7808A			SG140-08			SG7808			SG7808AC			SG340-08			SG7808C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	7.88		8.12	7.7		8.3	7.7		8.3	7.88		8.12	7.7		8.3	7.7		8.3	V
Line Regulation		T_J = 25°C, V_{IN} = 10.5 to 25V		8	40		8	80		8	80		8	80		8	80		16	160	mV
		T_J = 25°C, V_{IN} = 11 to 17V		4	20		4	40		4	40		4	40		4	40		8	80	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		24	70		24	80		24	80		24	80		24	80		40	160	mV
	P,R,K Pkg	T_J = 25°C, I_O = 250 to 750mA		8	35		8	40		8	40		8	40		8	40		16	80	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		8	35		8	40		8	40		8	40		8	40		16	80	mV
Total Output Voltage Tolerance V_{IN} = 11.5 to 23V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	7.76		8.24	7.6		8.4	7.6		8.4	7.6		8.24	7.6		8.4	7.6		8.4	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 11.5 to 25V			0.8			0.8			0.8			1.0			1.0			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2			2			2			2			2			2		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.5			2.5			2.5			2.5			2.5			2.5		A
		T_J = 25°C, T-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		1.8			1.8			1.8			1.8			1.8			1.8		A
		T_J = 25°C, T-Pkg		0.6			0.6			0.6			0.6			0.6			0.6		A
Temperature Coefficient		I_O = 5mA		−0.6			−0.6			−0.6			−0.6			−0.6			−0.6		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		72			72			72			72			72			72		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		52			52			52			52			52			52		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		32			32			32			32			32			32		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			1765			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 14V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7812A			SG140-12			SG7812			SG7812AC			SG340-12			SG7812C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	11.8		12.2	11.5		12.5	11.5		12.5	11.8		12.2	11.5		12.5	11.5		12.5	V
Line Regulation		T_J = 25°C, V_{IN} = 14.5 to 30V		12	60		12	120		12	120		12	120		12	120		24	240	mV
		V_{IN} = 16 to 22V		6	30		6	60		6	60		6	60		6	60		12	120	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		28	120		28	120		28	120		28	120		28	120		80	240	mV
	P,R,K Pkg	T_J = 25°C, I_O = 250 to 750mA		10	40		10	60		10	60		10	60		10	60		24	120	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		10	40		10	60		10	60		10	60		10	60		24	120	mV
Total Output Voltage Tolerance V_{IN} = 15.5 to 27V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	11.7		12.3	11.4		12.6	11.4		12.6	11.7		12.3	11.4		12.6	11.4		12.6	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 15 to 30V			0.8			0.8			0.8			1.0			1.0			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2.0			2.0			2.0			2.0			2.0			2.0		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.5			2.5			2.5			2.5			2.5			2.5		A
		T_J = 25°C, T-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		1.5			1.5			1.5			1.5			1.5			1.5		A
		T_J = 25°C, T-Pkg		0.5			0.5			0.5			0.5			0.5			0.5		A
Temperature Coefficient		I_O = 5mA		−0.8			−0.8			−0.8			−0.8			−0.8			−0.8		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		71			71			71			71			71			71		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		75			75			75			75			75			75		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		48			48			48			48			48			48		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 19V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7815A			SG140-15			SG7815			SG7815AC			SG340-15			SG7815C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	14.8		15.2	14.4		15.6	14.4		15.6	14.8		15.2	14.4		15.6	14.4		15.6	V
Line Regulation		T_J = 25°C, V_{IN} = 17.5 to 30V		15	75		15	150		15	150		15	150		15	150		30	300	mV
		V_{IN} = 20 to 26V		8	40		8	75		8	75		8	75		8	75		15	150	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		30	100		30	150		30	150		30	150		30	150		100	300	mV
		I_O = 250 to 750mA		12	50		12	75		12	75		12	75		12	75		30	150	mV
	T-Pkg	I_O = 5mA to 500mA		12	50		12	75		12	75		12	75		12	75		30	150	mV
Total Output Voltage Tolerance V_{IN} = 18.5 to 30V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	14.6		15.4	14.3		15.7	14.3		15.7	14.6		15.4	14.3		15.7	14.3		15.7	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 18.5 to 30V			0.8			0.8			0.8			1.0			1.0			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2			2			2			2			2			2		V
		T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.2			2.2			2.2			2.2			2.2			2.2		A
		T-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		1.3			1.3			1.3			1.3			1.3			1.3		A
		T-Pkg		0.4			0.4			0.4			0.4			0.4			0.4		A
Temperature Coefficient		I_O = 5mA		−1.0			−1.0			−1.0			−1.0			−1.0			−1.0		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		70			70			70			70			70			70		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		90			90			90			90			90			90		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		60			60			60			60			60			60		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 23V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7818A			SG140-18			SG7818			SG7818AC			SG340-18			SG7818C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	17.7		18.3	17.3		18.7	17.3		18.7	17.7		18.3	17.3		18.7	17.3		18.7	V
Line Regulation		T_J = 25°C, V_{IN} = 21 to 33V		20	90		20	180		20	180		20	180		20	180		40	360	mV
		V_{IN} = 24 to 30V		20	45		10	90		10	90		10	90		10	90		20	180	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		40	120		40	180		40	180		40	180		40	180		120	360	mV
		I_O = 250 to 750mA		15	60		15	90		15	90		15	90		15	90		40	180	mV
	T-Pkg	I_O = 5mA to 500mA		15	60		15	90		15	90		15	90		15	90		40	180	mV
Total Output Voltage Tolerance V_{IN} = 22 to 33V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	17.5		18.5	17.1		18.9	17.1		18.9	17.5		18.5	17.1		18.9	17.1		18.9	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 22 to 33V			0.8			0.8			0.8			1.0			1.0			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2.0			2.0			2.0			2.0			2.0			2.0		V
		T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.2			2.2			2.2			2.2			2.2			2.2		A
		T-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
		T-Pkg		0.3			0.3			0.3			0.3			0.3			0.3		A
Temperature Coefficient		I_O = 5mA		−1.2			−1.2			−1.2			−1.2			−1.2			−1.2		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		69			69			69			69			69			69		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		110			110			110			110			110			110		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		72			72			72			72			72			72		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 27V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS	SG7820A	SG140-20	SG7820	SG7820AC	SG340-20	SG7820C	
PACKAGE STYLES (P/N SUFFIX)	K,R,T	K,R,T	K,R,T	K,P,R,T	K,P,R,T	K,P,R,T	
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)	−55°C to +150°C	−55°C to 150°C	−55°C to 150°C	0°C to 125°C	0°C to 125°C	0°C to 125°C	

PARAMETERS	TEST CONDITIONS (See notes below)		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage	T_J = 25°C		19.7		20.3	19.2		20.8	19.2		20.8	19.7		20.3	19.2		20.8	19.2		20.8	V
Line Regulation	T_J = 25°C	V_{IN} = 23 to 35V		22	100		22	200		22	200		22	200		22	200		44	400	mV
		V_{IN} = 26 to 32V		12	50		12	100		12	100		12	100		12	100		24	200	mV
Load Regulation P,R,K Pkg	T_J = 25°C	I_O = 5mA to 1.5A		45	140		45	200		45	200		45	200		45	200		150	400	mV
		I_O = 250 to 750mA		20	70		20	100		20	100		20	100		20	100		50	200	mV
Load Regulation T-Pkg	T_J = 25°C	I_O = 5mA to 500mA		20	70		20	100		20	100		20	100		20	100		50	200	mV
Total Output Voltage Tolerance V_{IN} = 24 to 35V	K-Pkg: I_O = 5 to 1500mA, P ≤ 20W		19.4		20.6	19.0		21.0	19.0		21.0	19.4		20.6	19.0		21.0	19.0		21.0	V
	R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																				
	T-Pkg: I_O = 5 to 500mA, P ≤ 2W																				
Quiescent Current	T_J = 25°C			4	6		4	6		4	6		4	6		4	8		4	8	mA
	Over Temperature Range				7			7			7			7			8.5			8.5	mA
Quiescent Current Change	With line: V_{IN} = 24 to 35V				0.8			0.8			0.8			1.0			1.0			1.0	mA
	With load: I_O = 5 to 1000mA				0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV	T_J = 25°C	K,R,P-Pkg: I_O = 1A		2.0			2.0			2.0			2.0			2.0			2.0		V
		T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current	T_J = 25°C	K,R,P-Pkg		2.2			2.2			2.2			2.2			2.2			2.2		A
		T-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
Short Circuit Current	T_J = 25°C	K,R,P-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
		T-Pkg		0.2			0.2			0.2			0.2			0.2			0.2		A
Temperature Coefficient	I_O = 5mA			−1.3			−1.3			−1.3			−1.3			−1.3			−1.3		mV /°C
Ripple Rejection	T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V			68			68			68			68			68			68		dB
Output Noise Voltage	T_J = 25°C, f = 10Hz to 100 kHz			140			140			140			140			140			140		μV rms
Long Term Stability	1000 hrs. at T_J = 125°C			80			80			80			80			80			80		mV
Thermal Shutdown	I_O = 5mA			175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 29V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7824A			SG140-24			SG7824			SG7824AC			SG340-24			SG7824C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	23.6		24.4	23.0		25.0	23.0		25.0	23.6		24.4	23.0		25.0	23.0		25.0	V
Line Regulation		T_J = 25°C, V_{IN} = 27 to 38V		25	120		25	240		25	240		25	240		25	240		50	480	mV
		T_J = 25°C, V_{IN} = 30 to 36V		14	60		14	120		14	120		14	120		14	120		28	240	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		50	160		50	240		50	240		50	240		50	240		180	480	mV
		T_J = 25°C, I_O = 250 to 750mA		25	80		25	120		25	120		25	120		25	120		70	240	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		25	80		25	120		25	120		25	120		25	120		70	240	mV
Total Output Voltage Tolerance V_{IN} = 28 to 38V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	23.3		24.7	22.8		25.2	22.8		25.2	23.3		24.7	22.8		25.2	22.8		25.2	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 28 to 38V			0.8			0.8			0.8			1.0			1.0			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2.0			2.0			2.0			2.0			2.0			2.0		V
		T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.2			2.2			2.2			2.2			2.2			2.2		A
		T-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		0.7			0.7			0.7			0.7			0.7			0.7		A
		T-Pkg		0.2			0.2			0.2			0.2			0.2			0.2		A
Temperature Coefficient		I_O = 5mA		−1.5			−1.5			−1.5			−1.5			−1.5			−1.5		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		66			66			66			66			66			66		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		170			170			170			170			170			170		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		96			96			96			96			96			96		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 33V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 40V

Three Terminal Negative Regulators

SG7900A / 7900AC
SG120 / 220 / 320
SG7900 / 7900C

1

DESCRIPTION

The SG7900A/7900/120/220/320 series of negative regulators offer self-contained, fixed-voltage capability with up to 1.5 amps of load current. With a variety of output voltages and four package options, this regulator series is an optimum complement to the SG7800A/7800/140/240/340 line of three terminal regulators.

These units feature a unique on-chip trimming system which allows the SG7900A series to be specified with an output voltage tolerance of ±1.5%. The SG7900A versions also offer much improved line regulation characteristics.

All protective features of thermal shutdown, current limiting, and safe-area control have been designed into these units and since these regulators require only a single output capacitor for satisfactory performance, ease of application is assured.

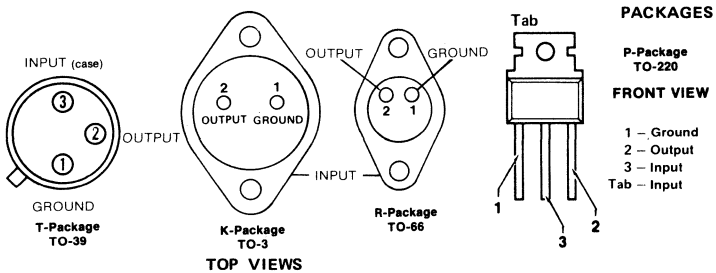
Although designed as fixed-voltage regulators, the output voltage can be increased through the use of a simple voltage divider. The low quiescent drain current of the device insures good regulation when this method is used.

These devices are available in hermetically sealed TO-3, TO-39 and TO-66 power packages as well as the plastic commercial power TO-220 package.

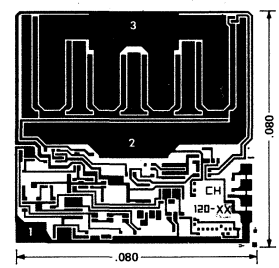
FEATURES

- **Output voltages set internally to ±1.5% (SG7900A)**
- **Output current to 1.5 amp**
- **Excellent line and load regulation**
- **Foldback current limiting**
- **Thermal overload protection**
- **Voltages available — −5 V, −5.2V, −8V, −12V, −15V, −18V, −20V**

CONNECTION DIAGRAMS



CHIP LAYOUT



ABSOLUTE MAXIMUM RATINGS

Device Output Voltage	Input Voltage	Input-Output Differential
−5V	−25V	25V
−5.2V	−25V	25V
−8 V	−35V	30V
−12V	−35V	30V
−15V	−40V	30V
−18V	−40V	30V
−20V	−40V	35V

Operating Junction Temperature Range

SG7900A/7900/120 ..... −55° C to +150° C
SG220 ..... 0° C to +150° C
SG7900AC/7900/320 ..... 0° C to +125° C

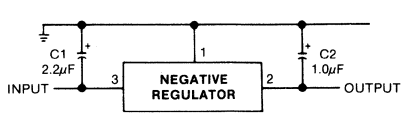
Storage Temperature Range ..... −65° C to +150° C
Lead Temperature (Soldering, 10 Sec) ..... +300° C

Power/Thermal Characteristics

Package	K (TO-3)	R (TO-66)	P (TO-220)	T (TO-39)
25° C Case Rated Power	20W	15W	15W	2W
25° C Ambient Rated Power	4.3W	3.0W	2.0W	1.0W
Design Current	1.5A	1.5A	1.0A	0.5A
Therm. Res θ_{JC} (°C/W)	3.0	5.0	3.0	15
θ_{JA} (°C/W)	35	40	60	120

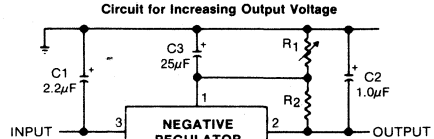
APPLICATIONS

Fixed Output Regulator



NOTE: 1. C1 is required only if regulator is separated from rectifier filter.
2. Both C1 and C2 should be low E.S.R. types such as solid tantalum. If aluminum electrolitics are used, at least 10 times values shown should be selected.
3. If large output capacities are used, the regulators must be protected from momentary input shorts. A high current diode from output to input will suffice.

Circuit for Increasing Output Voltage



NOTE: C3 optional for improved transient response and ripple rejection.

$$V_{OUT} = V\,(REGULATOR)\,\frac{R_1 + R_2}{R_1} \qquad R_2 = \frac{V(REG)}{15mA}$$

DEVICE PART NUMBERS			SG7905A			SG120-05			SG7905			SG7905AC			SG320-05			SG7905C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	−4.92		−5.08	−4.9		−5.1	−4.8		−5.2	−4.92		−5.08	−4.8		−5.2	−4.8		−5.2	V
Line Regulation		T_J = 25°C, V_{IN} = −7 to −25V		5	25		5	25		5	50		5	40		5	40		10	50	mV
		T_J = 25°C, V_{IN} = −8 to −12V		3	15		3	15		3	25		3	25		3	25		5	30	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		15	50		15	50		15	50		15	100		15	100		15	100	mV
		T_J = 25°C, I_O = 250 to 750mA		15	25		5	25		5	25		5	50		5	50		5	50	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		5	40		5	50		5	50		5	50		5	50		5	100	mV
Total Output Voltage Tolerance V_{IN} = −8 to −20V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	−4.85		−5.15	−4.8		−5.2	−4.70		−5.30	−4.85		−5.15	−4.75		−5.25	−4.75		−5.25	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		1	2		1	2		1	2		1	2		1	2		1	2	mA
		Over Temperature Range			2.5			2.5			2.5			2.5			2.5			3	mA
Quiescent Current Change		With line: V_{IN} = −8 to −25V			1.3			0.4			1.3			1.3			0.4			1.3	mA
		With load: I_O = 5 to 1000mA			0.5			0.4			0.5			0.5			0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2.0			2.0			2.0			2.0			2.0			2.0		V
		T_J = 25°C, T-Pkg: I_O = 500mA		2.0			2.0			2.0			2.0			2.0			2.0		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.5			2.5			2.5			2.5			2.5			2.5		A
		T_J = 25°C, T-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		2.1			2.1			2.1			2.1			2.1			2.1		A
		T_J = 25°C, T-Pkg		0.7			0.7			0.7			0.7			0.7			0.7		A
Temperature Coefficient		I_O = 5mA		−0.4			−0.4			−0.4			−0.4			−0.4			−0.4		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		60			60			60			60			60			60		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		100			100			100			100			100			100		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		20			20			20			20			20			20		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = −10V and I_O = 500mA for K,R,P-Package; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −25V.

DEVICE PART NUMBERS	SG7905.2A	SG120-5.2	SG7905.2	SG7905.2AC	SG320-5.2	SG7905.2C	
PACKAGE STYLES (P/N SUFFIX)	K,R,T	K,R,T	K,R,T	K,P,R,T	K,P,R,T	K,P,R,T	
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)	−55°C to +150°C	−55°C to 150°C	−55°C to 150°C	0°C to 125°C	0°C to 125°C	0°C to 125°C	

PARAMETERS	TEST CONDITIONS (See notes below)		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage	T_J = 25°C		-5.12		-5.28	−5.1		−5.3	−5.0		−5.4	-5.12		-5.28	−5.0		−5.4	−5.0		−5.4	V
Line Regulation	T_J = 25°C	V_{IN} = −8 to −25V		5	25		5	25		5	50		5	40		5	40		10	50	mV
		V_{IN} = −9 to −13V		3	15		3	15		3	25		3	25		3	25		5	30	mV
Load Regulation P,R,K Pkg	T_J = 25°C	I_O = 5mA to 1.5A		15	60		15	60		15	60		15	100		15	100		15	100	mV
		I_O = 250 to 750mA		5	30		5	30		5	30		5	50		5	50		5	50	mV
Load Regulation T-Pkg	T_J = 25°C	I_O = 5mA to 500mA		5	50		5	50		5	50		5	50		5	50		5	100	mV
Total Output Voltage Tolerance V_{IN} = −9 to −21V	K-Pkg: I_O = 5 to 1500mA, P ≤ 20W		-5.05		-5.35	-5.00		−5.40	−4.90		−5.50	-5.05		−5.35	−4.95		−5.45	−4.95		−5.45	V
	R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																				
	T-Pkg: I_O = 5 to 500mA, P ≤ 2W																				
Quiescent Current	T_J = 25°C			1	2		1	2		1	2		1	2		1	2		1	2	mA
	Over Temperature Range				2.5			2.5			2.5			2.5			2.5			3.0	mA
Quiescent Current Change	With line: V_{IN} = −9 to −25V				1.3			0.4			1.3			1.3			0.4			1.3	mA
	With load: I_O = 5 to 1000mA				0.5			0.4			0.5			0.5			0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV	T_J = 25°C	K,R,P-Pkg: I_O = 1A		1.8			1.8			1.8			1.8			1.8			1.8		V
		T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current	T_J = 25°C	K,R,P-Pkg		2.5			2.5			2.5			2.5			2.5			2.5		A
		T-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
Short Circuit Current	T_J = 25°C	K,R,P-Pkg		2.0			2.0			2.0			2.0			2.0			2.0		A
		T-Pkg		0.6			0.6			0.6			0.6			0.6			0.6		A
Temperature Coefficient	I_O = 5mA			−0.5			−0.5			−0.5			−0.5			−0.5			−0.5		mV /°C
Ripple Rejection	T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V			60			60			60			60			60			60		dB
Output Noise Voltage	T_J = 25°C, f = 10Hz to 100 kHz			125			125			125			125			125			125		μV rms
Long Term Stability	1000 hrs. at T_J = 125°C			24			24			24			24			24			24		mV
Thermal Shutdown	I_O = 5mA			175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = −10V and I_O = 500mA for K,R,P-Package; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −25V.

DEVICE PART NUMBERS			SG7908A			SG120-08			SG7908			SG7908AC			SG320-08			SG7908C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	-7.88		-8.12	-7.8		-8.2	-7.7		-8.3	-7.88		-8.12	-7.7		-8.3	-7.7		-8.3	V
Line Regulation		T_J = 25°C, V_{IN} = −10.5 to −25V		6	25		6	25		6	80		6	40		6	40		12	80	mV
		T_J = 25°C, V_{IN} = −11 to −17V		4	15		4	15		4	40		4	25		4	25		8	50	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		20	80		20	80		20	80		20	100		20	100		20	160	mV
		T_J = 25°C, I_O = 250 to 750mA		10	40		10	40		10	40		10	50		10	50		10	80	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		10	25		10	25		10	80		10	40		10	40		10	160	mV
Total Output Voltage Tolerance V_{IN} = −11.5 to −23V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	-7.76		-8.24	-7.65		-8.35	-7.60		-8.40	-7.76		-8.24	-7.60		-8.40	-7.60		-8.40	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		1	2		1	2		1	2		1	2		1	2		1	2	mA
		Over Temperature Range			2.5			2.5			2.5			2.5			2.5			2.5	mA
Quiescent Current Change		With line: V_{IN} = −11.5 to −25V			1.0			0.4			1.0			1.0			0.4			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.4			0.5			0.5			0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		1.1			1.1			1.1			1.1			1.1			1.1		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.0			1.0			1.0			1.0			1.0			1.0		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.5			2.5			2.5			2.5			2.5			2.5		A
		T_J = 25°C, T-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		1.5			1.5			1.5			1.5			1.5			1.5		A
		T_J = 25°C, T-Pkg		0.5			0.5			0.5			0.5			0.5			0.5		A
Temperature Coefficient		I_O = 5mA		−0.6			−0.6			−0.6			−0.6			−0.6			−0.6		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		60			60			60			60			60			60		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		175			175			175			175			175			175		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		32			32			32			32			32			32		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = −14V and I_O = 500mA for K,R,P-Package; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −35V.

DEVICE PART NUMBERS			SG7912A			SG120-12			SG7912			SG7912AC			SG320-12			SG7912C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	−11.8		−12.2	−11.7		−12.3	−11.5		−12.5	−11.8		−12.2	−11.6		−12.4	−11.5		−12.5	V
Line Regulation		T_J = 25°C, V_{IN} = −14.5 to −30V		6	25		6	25		6	80		6	50		6	50		12	80	mV
		T_J = 25°C, V_{IN} = −16 to −22V		4	15		4	15		4	50		4	30		4	30		8	50	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		20	80		20	80		20	120		20	80		20	80		20	240	mV
	P,R,K Pkg	T_J = 25°C, I_O = 250 to 750mA		10	40		10	40		10	60		10	40		10	40		10	120	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		10	25		10	25		10	120		10	40		10	40		10	240	mV
Total Output Voltage Tolerance V_{IN} = −15.5 to −27V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	−11.7		−12.3	−11.5		−12.5	−11.4		−12.6	−11.7		−12.3	−11.4		−12.6	−11.4		−12.6	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		3			3			3			3			3			3		mA
		Over Temperature Range			4			4			4			4			4			4	mA
Quiescent Current Change		With line: V_{IN} = −15 to −30V			1.0			0.4			1.0			1.0			0.4			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.4			0.5			0.5			0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		1.1			1.1			1.1			1.1			1.1			1.1		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.1			1.1			1.1			1.1			1.1			1.1		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.5			2.5			2.5			2.5			2.5			2.5		A
		T_J = 25°C, T-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		1.5			1.5			1.5			1.5			1.5			1.5		A
		T_J = 25°C, T-Pkg		0.5			0.5			0.5			0.5			0.5			0.5		A
Temperature Coefficient		I_O = 5mA		−0.8			−0.8			−0.8			−0.8			−0.8			−0.8		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		60			60			60			60			60			60		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		200			200			200			200			200			200		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		48			48			48			48			48			48		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = −19V and I_O = 500mA for K,R,P-Package; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −35V.

DEVICE PART NUMBERS			SG7915A			SG120-15			SG7915			SG7915AC			SG320-15			SG7915C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	−14.8		−15.2	−14.7		−15.3	−14.4		−15.6	−14.8		−15.2	−14.6		−15.4	−14.4		−15.6	V
Line Regulation		T_J = 25°C, V_{IN} = −17.5 to −30V		6	25		6	25		6	80		6	50		6	50		12	80	mV
		T_J = 25°C, V_{IN} = −20 to −26V		4	15		4	15		4	50		4	30		4	30		8	50	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		20	180		20	80		20	150		20	180		20	80		20	300	mV
	P,R,K Pkg	T_J = 25°C, I_O = 250 to 750mA		10	40		10	40		10	75		10	40		10	40		10	150	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		10	25		10	25		10	120		10	40		10	40		10	240	mV
Total Output Voltage Tolerance V_{IN} = −18.5 to −30V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	−14.6		−15.4	−14.5		−15.5	−14.3		−15.7	−14.6		−15.4	−14.4		−15.6	−14.3		−15.7	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		3			3			3			3			3			3		mA
		Over Temperature Range			4			4			4			4			4			4	mA
Quiescent Current Change		With line: V_{IN} = −18.5 to −30V			1.0			0.4			1.0			1.0			0.4			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.4			0.5			0.5			0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		1.1			1.1			1.1			1.1			1.1			1.1		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.1			1.1			1.1			1.1			1.1			1.1		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.2			2.2			2.2			2.2			2.2			2.2		A
		T_J = 25°C, T-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		1.3			1.3			1.3			1.3			1.3			1.3		A
		T_J = 25°C, T-Pkg		0.4			0.4			0.4			0.4			0.4			0.4		A
Temperature Coefficient		I_O = 5mA		−0.9			−0.9			−0.9			−0.9			−0.9			−0.9		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		60			60			60			60			60			60		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		250			250			250			250			250			250		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		60			60			60			60			60			60		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = −23V and I_O = 500mA for K,R,P-Package; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −35V.
7. Line regulation @ I_O = 5mA = 10mV (120-12) and 20mV (320-12).

DEVICE PART NUMBERS			SG7918A			SG120-18			SG7918			SG7918AC			SG320-18			SG7918C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	−17.7		−18.3	−17.6		−18.4	−17.3		−18.7	−17.7		−18.3	−17.4		−18.6	−17.4		−18.6	V
Line Regulation		T_J = 25°C, V_{IN} = −21 to −33V		6	25		6	25		6	180		6	50		6	50		12	80	mV
		T_J = 25°C, V_{IN} = −24 to −30V		4	15		4	15		4	50		4	30		4	30		8	50	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		20	80		20	80		20	180		20	80		20	80		20	360	mV
	P,R,K Pkg	T_J = 25°C, I_O = 250 to 750mA		10	40		10	40		10	90		10	40		10	40		10	180	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		10	25		10	25		10	150		10	40		10	40		10	300	mV
Total Output Voltage Tolerance V_{IN} = −22 to −33V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	−17.5		−18.5	−17.4		−18.6	−17.1		−18.9	−17.5		−18.5	−17.1		−18.9	−17.1		−18.9	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		3			3			3			3			3			3		mA
		Over Temperature Range			4			4			4			4			4			4	mA
Quiescent Current Change		With line: V_{IN} = −22 to −33V			1.0			0.4			1.0			1.0			0.4			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.4			0.5			0.5			0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		1.1			1.1			1.1			1.1			1.1			1.1		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.1			1.1			1.1			1.1			1.1			1.1		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.2			2.2			2.2			2.2			2.2			2.2		A
		T_J = 25°C, T-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		1.1			1.1			1.1			1.1			1.1			1.1		A
		T_J = 25°C, T-Pkg		0.3			0.3			0.3			0.3			0.3			0.3		A
Temperature Coefficient		I_O = 5mA		−1.0			−1.0			−1.0			−1.0			−1.0			−1.0		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		60			60			60			60			60			60		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		300			300			300			300			300			300		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		72			72			72			72			72			72		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = −27V and I_O = 500mA for K,R,P-Package; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −35V.

DEVICE PART NUMBERS			SG7920A			SG120-20			SG7920			SG7920AC			SG320-20			SG7920C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	−19.7		−20.3	−19.5		−18.5	−19.2		−20.8	−19.7		−20.3	−19.2		−20.8	−19.2		−20.8	V
Line Regulation		T_J = 25°C, V_{IN} = −23 to −35V		6	25		6	25		6	80		6	50		6	50		12	80	mV
		T_J = 25°C, V_{IN} = −26 to −32V		4	15		4	15		4	50		4	30		4	30		8	50	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		20	80		20	80		20	200		20	80		20	80		20	400	mV
		T_J = 25°C, I_O = 250 to 750mA		10	40		10	40		10	100		10	40		10	40		10	200	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		10	25		10	25		10	150		10	40		10	80		10	300	mV
Total Output Voltage Tolerance V_{IN} = −24 to −35V		K-Pkg: I_O = 5 to 1500mA, P ≤ 20W	−19.4		−20.6	−19.3		−20.7	−19.0		−21.0	−19.4		−20.6	−19.0		−21.0	−19.0		−21.0	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		3			3			3			3			3			3		mA
		Over Temperature Range			4			4			4			4			4			4	mA
Quiescent Current Change		With line: V_{IN} = −24 to −35V			1.0			0.4			1.0			1.0			0.4			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.4			0.5			0.5			0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		1.1			1.1			1.1			1.1			1.1			1.1		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.1			1.1			1.1			1.1			1.1			1.1		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.2			2.2			2.2			2.2			2.2			2.2		A
		T_J = 25°C, T-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
		T_J = 25°C, T-Pkg		0.2			0.2			0.2			0.2			0.2			0.2		A
Temperature Coefficient		I_O = 5mA		−1.1			−1.1			−1.1			−1.1			−1.1			−1.1		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		60			60			60			60			60			60		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		350			350			350			350			350			350		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		80			80			80			80			80			80		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = −29V and I_O = 500mA for K,R,P-Package; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −35V.
7. Line regulation @ I_O = 5mA = 20mV (120-20) and 36mV (320-20).

OPERATIONAL AMPLIFIERS

General Purpose, Compensated Op Amps

General Purpose, Uncompensated Op Amps

Dual, Compensated Op Amps

Quad Op Amps

High Performance Op Amps

High Voltage Op Amps

Low Power Op Amps

Voltage Followers

High Performance Quad Op Amp

SG101/201

The SG101/201 are general purpose operational amplifiers. Features include excellent input bias/current and drift characteristics plus short circuit protection and pin compatibility with many industry-standard operational amplifiers.

- **Frequency compensated with a single capacitor — no resistor required**
- **Low current drain: 1.8mA at±20V**
- **Continuous short circuit protection**
- **Operation as a comparator with differential inputs as high as±30V**
- **No latch up when common mode range is exceeded**

SG101A/201A/301A

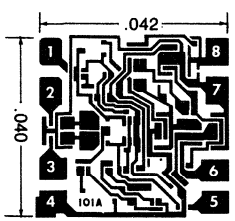
The SG101A/201A/301A offer improved performance over the SG101/201 operational amplifiers and also provide short circuit protection and pin compatibility with industry standard types.

- **3mV offset voltage over temperature**
- **100nA input current over temperature**
- **20nA offset current over temperature**
- **Guaranteed drift characteristics**
- **Offsets guaranteed over full common mode range**

PARAMETERS*	101	201	101A	201A	301A	UNITS
Supply Voltage	±5 to ±20	±5 to ±20	±5 to ±20		±5 to ±15	V
Operating Temperature Range	−55 to +125	0 to +70	−55 to +125	−25 to +85	0 to +70	°C
Package Types	T, Y, J, F	T,Y,J,F,N,M	T, Y, J, F	T, Y, J, F, N, M		–
Input Offset Voltage	5.0	7.5	2.0 (3.0)		7.5 (10)	mV
Input Offset Current	200 (500)	500 (750)	10 (20)		50 (70)	nA
Input Bias Current	0.5 (1.5)	1.5 (2.0)	0.075 (0.1)		0.25 (0.30)	μA
Temp Coeff Input Offset Voltage	(3.0 typ)	(6.0 typ)	15		30	μV/°C
Temp Coeff INput Offset Current	–	–	0.2		0.6	nA/°C
Large Signal Voltage Gain[1]	50 (25)	20 (15)	50 (25)		25 (15)	V/mV
Common Mode Rejection	(70)	(65)	(80)		(80)	dB
Power Supply Rejection	(316)	(316)	(100)		(100)	μV/V
Input Common Mode Voltage Range[2]	(±12)	(±12)	(+15, −12)		(+15, −12)	V
Differential Input Voltage	±30	±30	±30		±30	V
Slew Rate A_V = 1,	0.2	0.2	0.2		0.2	V/μS
A_V = 10	3 (typ)	3 (typ)	3 (typ)		3 (typ)	
Unity Gain Bandwidth	0.5 (typ)	0.5 (typ)	0.5 (typ)		0.5 (typ)	MHz
Supply Current	3.0	3.0	3.0		3.0	mA
V_{out} R_L = 2kΩ	±10	±10	±10		±10	V
R_L = 10kΩ	±12	±12	±12		±12	V
Noise						
R_S = 1kΩ f = 10Hz to 10kHz	4	4	4		4	μV(rms)
R_S = 500kΩ f = 10Hz to 10kHz	25	25	25		25	(typ)

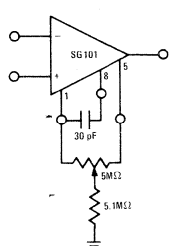
*Parameters apply over supply voltage range and are min./max. limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

[1] R_L = 2kΩ [2] V_S = ±15V

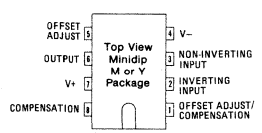


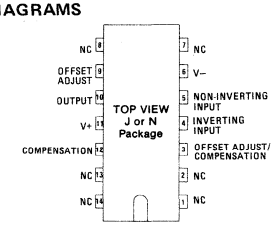
SG101/201, SG101A/201A/301A Chip
(See T-package diagram for pad functions)

Compensation and Optional Balancing Circuit



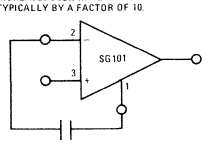
CONNECTION DIAGRAMS

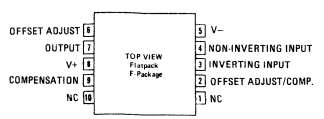


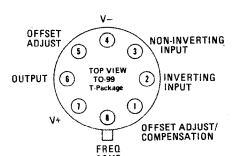


Feedforward Compensation

INCREASES SLEW RATE AND GAIN-BANDWIDTH TYPICALLY BY A FACTOR OF 10.







SG102/202/302

The SG102/202/302 are high-gain operational amplifiers designed specifically for unity-gain non-inverting voltage follower applications. The devices incorporate advanced super-beta transistor processing techniques to obtain very low input current and high input impedance. The input transisters are operated at zero collector-base voltage to virtually eliminate high temperature leakage currents resulting in extremely low input current and low offset voltage drift.

- **Low input bias current – 100 nA**
- **High input resistance – 10,000MΩ**
- **Internal frequency compensation**
- **Fast slewing – 10V/μs – typ**
- **Simple offset balancing with 1k potentiometer**

SG110/210/310

The SG110/210/310 are high gain operational amplifiers internally connected as unity-gain non-inverting amplifiers. Super-beta transistors are used in the input stage to obtain extremely low bias currents without sacrificing speed. These devices are directly interchangeable with the 101, 102, 741 and 709 in voltage follower applications. Internal frequency compensation and offset balancing are provided. The SG110 family is useful in fast sample and hold circuits, active filters or as general purpose buffers.

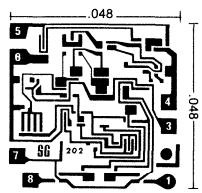
- **10nA input current max over temperature**
- **20MHz small signal bandwidth – typ**
- **30V/μs slew rate – typ**
- **±5V to ±18V supply voltage range**
- **No external frequency compensation necessary**

2

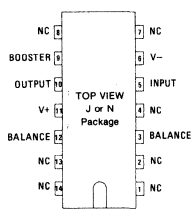
PARAMETERS*	102	202	302	110	210	310	UNITS
Supply Voltage	±15	±15	±15	±5 to ±18	±5 to ±18	±5 to ±18	V
Operating Temperature Range	–55 to +125	–25 to +85	0 to +70	–55 to +125	–25 to +85	0 to +70	°C
Package Types	T, J, Y	T, J, M, N, Y		T, J, Y	T, J, M, N, Y		
Input Offset Voltage	5.0 (7.5)	10 (15)	15 (20)	4.0 (6.0)	4.0 (6.0)	7.5 (10)	mV
Input Bias Current	10 (100)	15 (50)	30 (50)	3.0 (10)	3.0 (10)	7.0 (10)	nA
Temp Coeff Input Offset Voltage	6 (typ)	15 (typ)	20 (typ)	12 (typ)	6 (typ)	10 (typ)	μV/°C
Large Signal Voltage Gain	(0.999)	0.999	0.9985	0.999	0.999	0.999	V/V
Power Supply Rejection	60	60	60	70	70	70	dB
Input Common Mode Range	±10	±10	±10	±10	±10	±10	±10
Input Resistance	10^{10}	10^{10}	10^{9}	10^{10}	10^{10}	10^{10}	Ω
Output Resistance	2.5	2.5	2.5	2.5	2.5	2.5	Ω
V_{OS} Adjust	1kΩPot	1kΩPot	1kΩPot	1kΩPot	1kΩPot	1kΩPot	–
Slew Rate $A_V = 1$	10 (typ)	10 (typ)	10 (typ)	30 (typ)	30 (typ)	30 (typ)	V/μS
Unity Gain Bandwidth (typ, MHz)	8 (typ)	8 (typ)	8 (typ)	12 (typ)	12 (typ)	12 (typ)	MHz
Supply Current	5.5	5.5	5.5	5.5	5.5	5.5	mA
V_{out} $R_L = 10k\Omega$	±10	±10	±10	±10	±10	±10	V

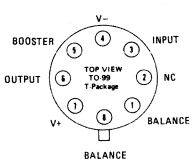
*Parameters apply over supply voltage range and are min./max. limits either at $T_A = 25°C$ (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

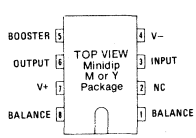
CONNECTION DIAGRAMS



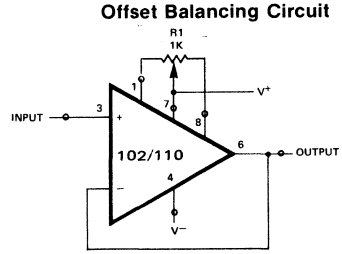
SG102/202/302, SG110/210/310 Chip (See T-package diagram for pad functions)



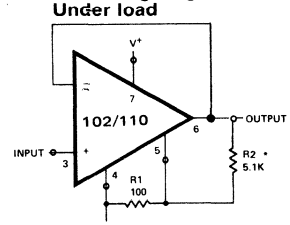




Offset Balancing Circuit



Increasing Negative Swing Under load



*May be added to reduce internal dissipation

SG107/207/307

The SG107/207/307 offer excellent input bias currents and drift characteristics as well as short circuit protection and pin compatibility with the 741 class of amplifiers.

- **3mV max offset voltage over temperature**
- **100 nA max input bias current over temperature**
- **20nA max offset current over temperature**
- **Offsets guaranteed over full common mode range**
- **Guaranteed drift characteristics**

SG741/741C

SG741/741C are pin compatible with the most widely accepted operational amplifiers and provide excellent performance for a wide range of applications.

- **Complete short circuit protection**
- **Offset voltage null capability**
- **High common mode voltage range**
- **High differential input voltage range**

SG1217/3217

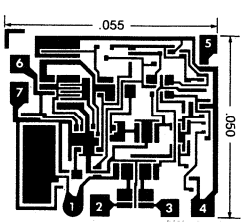
These devices are identical to the SG741/741C types, except internal compensation is reduced from 30pF to 3pF. Frequency response is ten times that of the standard device. Stability is unconditional from open loop to a closed loop gain of 20dB. These devices are especially useful in hybrid applications since higher bandpass is achieved without an outboard capacitor.

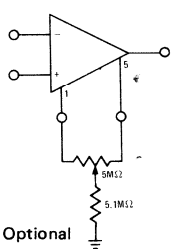
- **Slew rate typically 5V/μsec**
- **10 times frequency response 741/741C**
- **Ideal chip for hybrid applications**

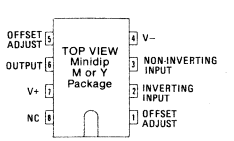
PARAMETERS*	107	207	307	741	741C	1217	3217	Units
Supply Voltage	±5 to ±20		±5 to ±20	±15	±15	±15	±15	V
Operating Temperature Range	−55 to +125	−25 to +85	0 to +70	−55 to +125	0 to +70	−55 to +125	0 to +70	°C
Package Types	T, J, F, Y	T, J, F, Y, M, N		T, J, F, Y	T,J,Y,F,M,N	T, J, F, Y	T,J,Y,F,M,N	–
Input Offset Voltage	2.0 (3.0)		7.5 (10)	5.0 (6.0)	6.0 (7.5)	5.0 (6.0)	6.0 (7.5)	mV
Input Offset Current	10 (20)		50 (70)	200 (500)	200 (300)	200 (500)	200 (500)	nA
Input Bias Current	0.075 (0.1)		0.25 (0.3)	0.5 (1.5)	0.5 (0.8)	0.5 (1.5)	0.5 (0.8)	μA
Temp. Coeff. Input Offset Voltage	(15)[2]		(30)[2]	(3.0 typ)	(6.0 typ)	(3.0 typ)	(6.0 typ)	μV/°C
Temp. Coeff. Input Offset Current	(0.2)		(0.6)	(0.5 typ)	(0.5 typ)	(0.5 typ)	(0.5 typ)	nA/°C
Large Signal Voltage Gain	50 (20)		25 (15)	50 (25)	20 (15)	50 (25)	20 (15)	V/mV
Common Mode Rejection	(80)		(80)	(70)	70	(70)	70	dB
Power Supply Rejection	(100)		(100)	(150)	150	(150)	150	μV/V
Input Common Mode Range	+15, −12		+15, −12	±12	±12	±12	±12	V
Differential Input Voltage	±30		±30	±30	±30	±30	±30	V
Unity Gain Bandwidth	0.5 (typ)		0.5 (typ)	0.8 (typ)	0.8 (typ)	0.8 (typ)	0.8 (typ)	MHz
Slew Rate	0.2		0.2	0.3	0.3	5.0 (typ)[3]	5.0 (typ)[3]	V/μS
Supply Current	3.0		3.0	2.8	2.8	2.8	2.8	mA
Output Voltage Swing								
R_L = 2kΩ	±10		±10	±10	±10	±10	±10	V
R_L = 10kΩ	±12		±12	±12		±12		V
Noise (typ)								
R_S = 1kΩ f = 10Hz to 10kHz	4		4	3	3	3	3	μV (rms) (typ)
R_S = 500kΩ f = 10Hz to 10kHz	25		25	25	25	25	25	

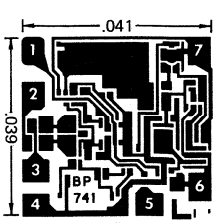
*Parameters apply over supply voltage range and are min./max. limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

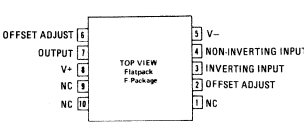
[1] V_S = ±15V [2] T_A = +25°C ≤ +125°C [3] Minimum recommended closed loop gain of 10.

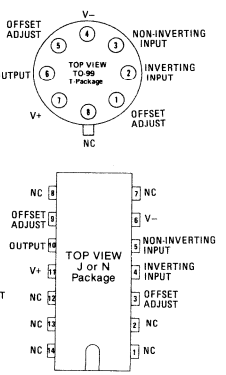


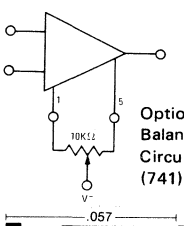


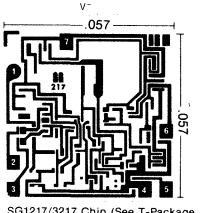












SG108/208/308 SG108A/208A/308A
SG1118/2118/3118 SG1118A/2118A/3118A

This series provides input currents and offset voltages which approach performance levels previously associated only with FET or chopper stabilized amplifiers. Superior power supply rejection ratio allows use of unregulated supplies and internal short circuit protection makes application nearly foolproof. Also, these devices feature low power consumption over a wide range of supply voltages. Frequency compensation for the 108 series is accomplished with a single external capacitor.

The SG1118 types are internally compensated versions of the 108 devices. Since a 30pF capacitor is built into the chip, no external components are needed for frequency compensation. In addition, provision is made for paralleling the internal capacitor making it possible to over-compensate to increase stability margin. The "A" versions are high performance selections from the 108 and 1118 types.

- **Extremely low input bias currents**
- **Offset currents less than 1.0nA**
- **Guaranteed voltage and current drift characteristics**
- **300μA power supply current**
- **Internal compensation on 1118/2118/3118 types**

2

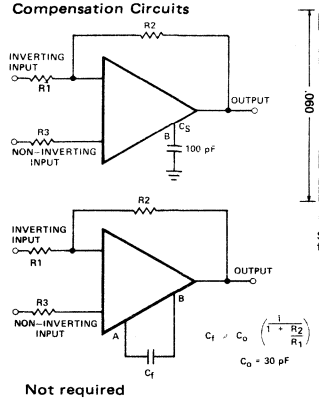
PARAMETERS*[1]	108/1118	208/2118	308/3118	108A/1118A	208A/2118A	308A/3118A	UNITS
Supply Voltage	±5 to ±20		±5 to ±15	±5 to ±20		±5 to ±15	V
Operating Temperature Range	–55 to +125	–25 to +85	0 to +70	–55 to +125	–25 to +85	0 to +70	°C
Package Types	J, Y, T, F	J, Y, T, F, M		J, Y, T, F	J, Y, T, F, M		–
Input Offset Voltage	2.0 (3.0)		7.5 (10)	0.5 (1.0)		0.5 (0.73)	mV
Input Offset Current	0.2 (0.4)		1.0 (1.5)	0.2 (0.4)		1.0 (1.5)	nA
Input Bias Current	2.0 (3.0)		7 (10)	2.0 (3.0)		7 (10)	nA
Temp Coeff Input Offset Voltage	(15)		(30)	(5.0)		(5.0)	μV/°C
Temp Coeff Input Offset Current	(2.5)		(10)	(2.5)		(10)	pA/°C
Large Signal Voltage Gain	50 (25)		25 (15)	80 (40)		80 (60)	V/mV
Common Mode Rejection	(85)		(80)	(96)		(96)	dB
Power Supply Rejection	(100)		(100)	(16)		(16)	μV/V
Input Common Mode Range	(±13.5)		(±13.5)	(±13.5)		(±13.5)	V
Slew Rate $A_V = 1$	0.1		0.1	0.1		0.1	V/μS
$A_V = 10$	3 (typ)		3 (typ)	3 (typ)		3 (typ)	
Unity Gain Bandwidth	0.3 (typ)		0.3 (typ)	0.3 (typ)		0.3 (typ)	MHz
Supply Current	0.6		0.8	0.6		0.8	mA
V_{out} $R_L = 10k\Omega$	±13		±13	±13		±13	V
Noise							
$R_s = 1k\Omega$ f = 10Hz to 10kHz	4		4	4		4	μV(rms) (typ)
$R_s = 500k\Omega$ f = 10Hz to 10kHz	20		20	20		20	

*Parameters apply over supply voltage range and are min./max. limits either at $T_A = 25°C$ (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

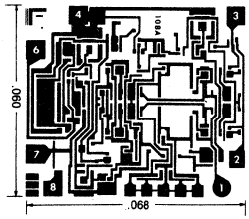
[1] Inputs are shunted with back-to-back diodes for overvoltage protection. Excessive current will flow if a differential input voltage in excess of one volt is applied between the inputs unless some limiting resistance is used.

CONNECTION DIAGRAMS

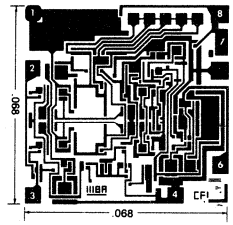
Compensation Circuits



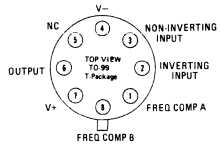
Not required for 1118/1118A

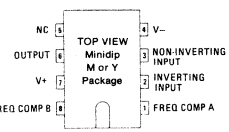


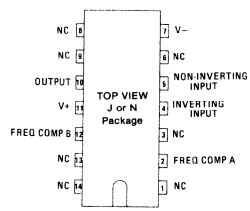
SG108/108A Chip (See T-package diagram for pad functions)

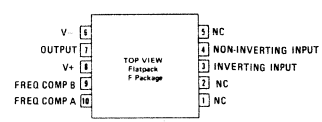


SG1118/1118A Chip (See T-package diagram for pad functions)









SG124/224/324

The SG124 series integrated circuit contains four true-differential, independent operational amplifiers. Each amplifier has been designed to operate from either a single supply voltage or plus and minus voltages and features internal frequency compensation, high gain, and very low supply current requirements. An additional significant advantage of these amplifiers is that when using a single supply, the input and output can be operated down to ground potential. Thus, they can be powered by a standard +5V DC logic supply and still be compatible with all forms of logic inputs and outputs.

- **Four internally compensated op amps in a single package**
- **Inputs and outputs can go to ground with a single supply voltage**
- **Input bias current is both low and constant with temperature**
- **Wide supply voltage compatibility with low current drain**
- **Available in 14-pin plastic or cerdip package**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V^+	$32V_{DC}$ or $\pm16V_{DC}$
Differential Input Voltage	$32V_{DC}$
Input Voltage	$-0.3V_{DC}$ to $+32V_{DC}$
Power Dissipation (Note 1)	
N Package (plastic)	600mW
Derate above 25°C	6.0mW/°C
J Package (cerdip)	1000mW
Derate above 25°C	6.7mW/°C
Output Short-Circuit to Gnd (Note 2) $V^+ \leq 15V_{DC}$ and $T_A = 25°C$	Continuous
Operating Temperature Range	
SG124	–55°C to +125°C
SG224	–25°C to +85°C
SG324	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

2

Electrical Characteristics ($V^+ = +5V$ DC and $T_A = 25°C$ unless otherwise noted)

Parameter	Conditions	SG124 Min.	SG124 Typ.	SG124 Max.	SG224/SG324 Min.	SG224/SG324 Typ.	SG224/SG324 Max.	Units
Input Offset Voltage	$R_S = 0\Omega$	—	2	5	—	2	7	mV_{DC}
Input Bias Current (Note 3)	$[I_{IN}(+) + I_{IN}(-)]/2$	—	45	300	—	45	500	nA_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$	—	±3	±30	—	±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 4)		0	—	V^+-1.5	0	—	V^+-1.5	V_{DC}
Supply Current	$R_L = \infty$ On All Op Amps	—	0.8	2	—	0.8	2	mA_{DC}
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	—	100	—	—	100	—	V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$	0	—	V^+-1.5	0	—	V^+-1.5	V_{DC}
Common Mode Rejection Ratio	DC	—	85	—	—	85	—	dB
Power Supply Rejection Ratio	DC	—	100	—	—	100	—	dB
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz (Input Referred)	—	–120	—	—	–120	—	dB
Output Current Source	$V_{IN}^+ = +1V_{DC}$, $V_{IN}^- = 0\ V_{DC}$	20	40	—	20	40	—	mA_{DC}
Output Current Sink	$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$	10	20	—	10	20	—	mA_{DC}

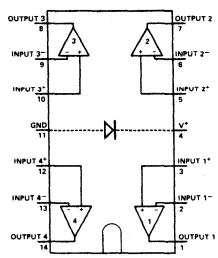
Note 1: For operating at high temperatures, the SG324 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The SG224 and SG124 can be derated based on a +150°C maximum junction temperature.

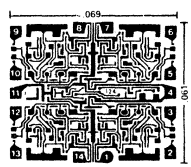
Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 3: The destruction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 4: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+-1.5V, but either or both inputs can go to $+30V_{DC}$ without damage.

CONNECTION DIAGRAM





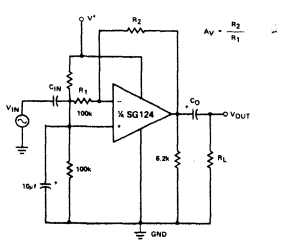
CHIP BONDING DIAGRAM

APPLICATIONS INFORMATION

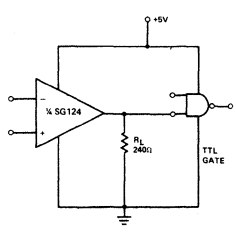
To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For AC applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in DC applications, there is no crossover distortion.

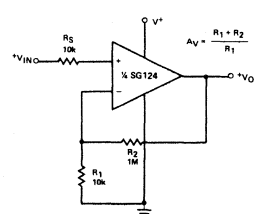
Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.



SINGLE SUPPLY INVERTING AC AMPLIFIER WITH INPUT BIASED TO ONE-HALF SUPPLY



TTL INTERFACE

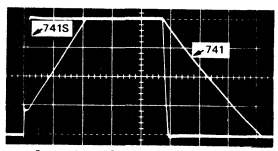


SINGLE SUPPLY NON-INVERTING DC AMPLIFIER (0V INPUT = 0V OUTPUT)

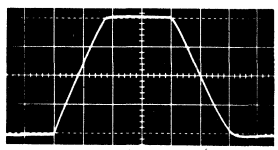
SG741S/SG741SC

The SG741S/741SC has been designed to provide a slew rate in excess of 20 times that of the popular SG741 circuit and yet be fully interchangeable in all other aspects. With input and output protection, internal compensation, and single-component offset nulling, this amplifier has all the features which have made the SG741 so easy to use. A guaranteed minimum slew rate of 10 volts per microsecond makes this device ideally suited for D to A converters and all applications requiring greater power bandwidth.

- **10 V/μs minimum slew rate**
- **Internally compensated**
- **Wide common mode and differential voltage range**
- **M, T, and Y Packages available**



Response Comparison, SG741S vs. SG741, 10μS/div., 5V/div.



Slew Rate, 1 μS/div., 5V/div.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

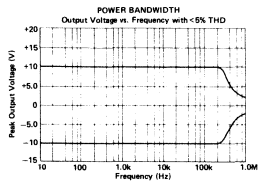
Rating	SG741S	SG741SC	Unit
Power Supply Voltage	+22 -22	+18 -18	Vdc
Differential Input Signal Voltage	±30		Volts
Common-Mode Input Voltage Swing (See Note 1)	±15		Volts
Output Short-Circuit Duration (See Note 2)	Continuous		
Power Dissipation (Package Limitation)			
T-Package- -TO-99 Metal Can	680		mW
Derate above T_A = +25°C	4.6		mW/°C
M-Package-Plastic Dual In-Line Minidip	625		mW
Derate above T_A = +25°C	5.0		mW/°C
Operating Temperature Range	-55 to +125	0 to +75	°C
Storage Temperature Range			°C
T-Package	-65 to +150		
M-Package	-55 to +125		

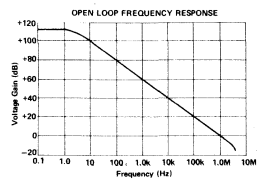
Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 Vdc.

TYPICAL CHARACTERISTICS

(V+ = +15 Vdc, V− = -15 Vdc, T_A = +25°C unless otherwise noted.)



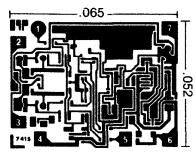


ELECTRICAL CHARACTERISTICS (V+ = +15 Vdc, V− = -15 Vdc, T_A = +25°C unless otherwise noted)

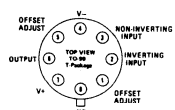
Characteristic	SG741S Min.	SG741S Typ.	SG741S Max.	SG741SC** Min.	SG741SC** Typ.	SG741SC** Max.	Unit
Power Bandwidth A_V = 1, R_L = 2.0 kΩ, THD = 5%, V_O = 20 V(p-p)	150	200	–	150	200	–	kHz
Large-Signal Transient Response (Slew Rate)							
V(–) to V(+)	10	20	–	10	20	–	V/μs
V(+) to V(–)	10	12	–	10	12	–	
Settling Time (to within 0.1%)	–	3.0	–	–	3.0	–	μs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV)							
Rise Time	–	0.25	–	–	0.25	–	μs
Fall Time	–	0.25	–	–	0.25	–	μs
Propagation Delay Time	–	0.25	–	–	0.25	–	μs
Overshoot	–	20	–	–	20	–	%
Short-Circuit Output Currents	±10	–	±35	±10	–	±35	mA
Open-Loop Voltage Gain (R_L = 2.0 kΩ)							–
V_O = ±10 V, T_A = +25°C	50,000	200,000	–	20,000	100,000	–	
V_O = ±10 V, T_A = T_{low}* to T_{high}*	25,000	–	–	15,000	–	–	
Output Impedance (f = 20 Hz)	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Swing							V_{pk}
R_L = 10 kΩ, T_A = +25°C	±12	±14	–	±12	±14	–	
R_L = 2.0 kΩ, T_A = +25°C	±10	±13	–	±10	±13	–	
R_L = 2.0 kΩ, T_A = T_{low} to T_{high}	±10	–	–	±10	–	–	
Input Common-Mode Voltage Swing	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz)	70	90	–	70	90	–	dB
Input Bias Current							μA
T_A = +25°C	–	0.2	0.5	–	0.2	0.5	
T_A = T_{low}	–	0.5	1.5	–	–	0.8	
Input Offset Current							μA
T_A = +25°C	–	0.03	0.2	–	0.03	0.2	
T_A = T_{low} to T_{high}	–	–	0.5	–	–	0.3	
Input Offset Voltage (R_S = ⩽ 10 kΩ)							mV
T_A = +25°C	–	1.0	5.0	–	2.0	6.0	
T_A = T_{low} to T_{high}	–	–	6.0	–	–	7.5	
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} to T_{high})							
R_S = 50Ω	–	3.0	–	–	3.0	–	μV/°C
R_S = 10 kΩ	–	6.0	–	–	6.0	–	
Average Temperature Coefficient of Input Offset Current (T_A = T_{low} to T_{high})	–	30	–	–	30	–	nA/°C
DC Power Dissipation (Power Supply = ±15 V, V_O = 0)	–	30	85	–	30	85	mW
Positive Voltage Supply Sensitivity (V– constant)	–	2.0	150	–	2.0	150	μV/V
Negative Voltage Supply Sensitivity (V+ constant)	–	10	150	–	10	150	μV/V

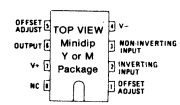
*T_{low} = 0 for SG741SC
= -55°C for SG741S
T_{high} = +75°C for SG741SC
= +125°C for SG741S

**Plastic Minidip (M-package) offered in limited temperature range device only



CONNECTION DIAGRAMS





SG747/747C

The SG747/747C are dual operational amplifiers offering performance which is identical to that of the 741/741C.

- **Complete short circuit protection**
- **Offset voltage null capability**
- **High common mode voltage range**
- **High differential input voltage range**

SG1558/1458

SG1558/1458 are internally compensated dual operational amplifiers intended for a wide range of analog applications where board space and/or weight are important. High common mode voltage range and absence of "latch-up" make these devices ideal for use as voltage followers. High gain and wide operating voltage range provide superior performance in integrator, summing amplifier and general feedback applications.

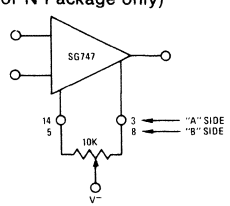
- **Internally compensated**
- **Short-circuit protected**
- **Low power consumption**
- **6dB/octave roll-off**
- **Minidip package**

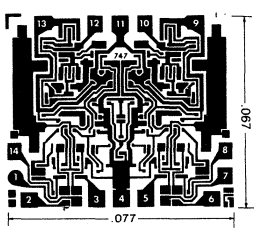
PARAMETERS*	747[2,5]	747C[2,5]	1558[2]	1458[2]	1458C[2]	Units
Supply Voltage	±15	±15	±15	±15	±15	V
Operating Temperature Range	−55 to +125	0 to +70	−55 to +125	0 to 75	0 to 75	°C
Package Types	T, J, N		T, M			–
Input Offset Voltage	5.0 (6.0)	6.0 (7.5)	5.0 (6.0)	6.0 (7.5)	10.0 (12.0)	mV
Input Offset Current	200 (500)	200 (300)	200 (500)	200 (300)	300 (400)	nA
Input Bias Current	0.5 (1.5)	0.5 (0.8)	0.5 (1.5)	0.5 (0.8)	0.7 (1.0)	μA
Temp Coeff Input Offset Voltage	(3.0 typ)	(6.0 typ)	(3.0 typ)	(6.0 typ)	(6.0 typ)	μV/°C
Temp Coeff Input Offset Current	(0.5 typ)	0.5 typ)	(0.5 typ)	(0.5 typ)	(0.5 typ)	nA/°C
Large Signal Voltage Gain	50 (25)[3]	20 (15)[3]	50 (25)[3]	20 (15)[3]	20 (15)[4]	V/mV
Common Mode Rejection	(70)	70	(70)	70	60	dB
Power Supply Rejection	(150)	150	(150)	150	30 typ	μV/V
Input Common Mode Range	±12[1]	±12[1]	±12[1]	±12[1]	±11[1]	V
Differential Input Voltage	±30	±30	±30	±30	±30	V
Unity Gain Bandwidth	0.8 (typ)	0.8 (typ)	0.8 (typ)	0.8 (typ)	0.8 (typ)	MHz
Slew Rate	0.3	0.3	0.3	0.3	0.3	V/μS
Supply Current	2.8[2]	2.8[2]	2.8[2]	2.8[2]	4.0[2]	mA
Output Voltage Swing R_L = 2kΩ	±10	±10	±10	±10	±9	V
R_L = 10kΩ	±12	——	±12	±12	±11	V
Noise						
R_S = 1kΩ f = 10Hz to 10kHz	3 (typ)	3 (typ)	3 (typ)	3 (typ)	3 (typ)	μV(rms)
R_S = 500kΩ f = 10Hz to 10kHz	25 (typ)	25 (typ)	25 (typ)	25 (typ)	25 (typ)	

*Parameters apply over supply voltage range and are min./max. limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

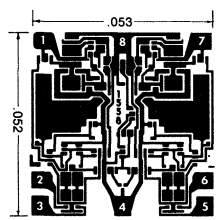
[1] V_S = ±15V [2] Each half [3] R_L = 2k [4] R_L = 10k [5] V + A and V + B are internally connected

Balancing Circuit (optional)
(J or N Package only)

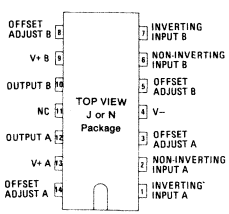


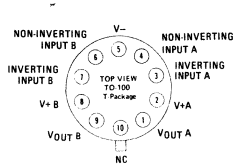


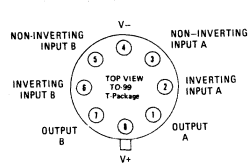
SG747/747C Chip (See 747J-Package for pad functions)

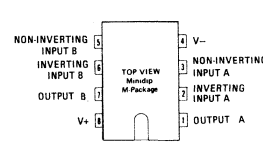


SG1558/1458 Chip (See 1558 M-Package for pad functions)









CONNECTION DIAGRAMS

SG748/748C

The SG748/748C are high performance devices which are similar to the 741/741C but without internal compensation. The 748/748C are functional and pin for pin replacements for the 301A and 201 type operational amplifiers.

- **Complete short circuit protection**
- **Offset voltage null capability**
- **High common mode voltage range**
- **High differential input voltage range**
- **Available in minidip**

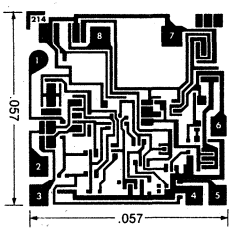
SG777/777C

The SG777/777C are precision operational amplifiers featuring low input offset current and low bias current. This device is available in most popular package styles, including minidip.

- **Low input bias current – 25nA**
- **Low input offset current – 3nA**
- **Low input offset voltage – 2mV**
- **Low offset voltage and current drift**
- **Short circuit protection**

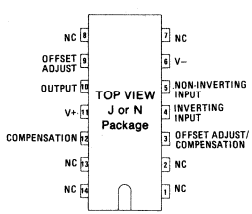
PARAMETERS*		748	748C	777	777C	UNITS
Supply Voltage		±15	±15	±15	±15	V
Operating Temperature Range		−55 to +125	0 to +70	−55 to +125	0 to +70	°C
Package Types		T, J, F, Y	T, J, F, Y, N, M	T, J, F, Y	T, Y, J, F, N, M	–
Input Offset Voltage		5.0 (6.0)	6.0 (7.5)	2.0 (3.0)	(5.0)	mV
Input Offset Current		200 (500)	200 (300)	3.0 (10.0)	20 (40)	nA
Input Bias Current		500 (1500)	500 (800)	25 (75)	100 (200)	nA
Temp Coeff Input Offset Voltage		(3.0 typ)	(6.0 typ)	15	30	µV/°C
Temp Coeff Input Offset Current		(0.5 typ)	(0.5 typ)	0.15	0.6	nA/°C
Large Signal Voltage Gain		50 (25)	25 (15)	50 (25)	25 (15)	V/mV
Common Mode Rejection		(70)	70	(80)	(70)	dB
Power Supply Rejection		(150)	150	(100)	(150)	µV/V
Input Common Mode Voltage Range		±12	±12	(±12)	(±12)	V
Differential Input Voltage		±30	±30	±30	±30	V
Slew Rate	A_V = 1,	0.3	0.3	0.5 (typ)	0.5 (typ)	V/µS
	A_V = 10	3 (typ)	3 (typ)	5.5 (typ)	5.5 (typ)	
Unity Gain Bandwidth (typ)		0.8	0.8	0.5	0.5	MHz
Supply Current		2.8	2.8	2.8	2.8	mA
V_{out}	R_L = 2kΩ	(±10)	±10	(±10)	(±10)	V
	R_L = 10kΩ	(±12)	––	(±12)	(±12)	V
Noise						
R_S = 1kΩ	f = 10Hz to 10kHz	4	4	4	4	µV(rms)
R_S = 500kΩ	f = 10Hz to 10kHz	25	25	25	25	typ

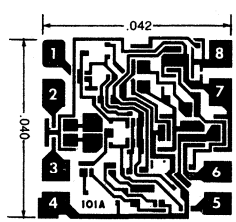
*Parameters apply over supply voltage range and are min./max. limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.



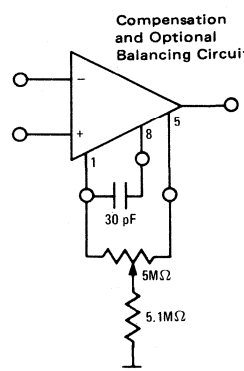
SG748/748C

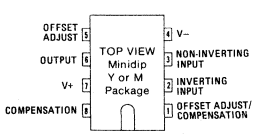
CONNECTION DIAGRAMS

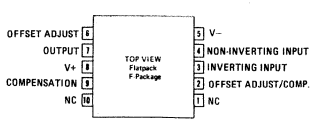


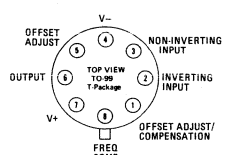


SG777/777C Chip









SG1250/SG2250/SG3250 — Single
SG1252/SG2252/SG3252 — Dual
SG1253/SG2253/SG3253 — Triple
SG4250/SG4250C — Single

ADVANCED DATA
Performance data described herein represent design goals. Final device specifications are subject to change.

DESCRIPTION

SG1250/1252/1253 operational amplifiers are single, dual, and triple operational amplifiers which have been designed to offer exceptional performance under conditions of extremely low internal power consumption. Quiescent current is determined by a single external resistor which permits operation over a wide range of currents and voltages.

FEATURES

- **Adjustable power consumption to less than 20 microwatts**
- **Supply voltages from ± 0.75 to ± 18 volts**
- **Less than 15 nA bias currents**
- **Complete short-circuit protection**
- **Internally compensated**

DESCRIPTION

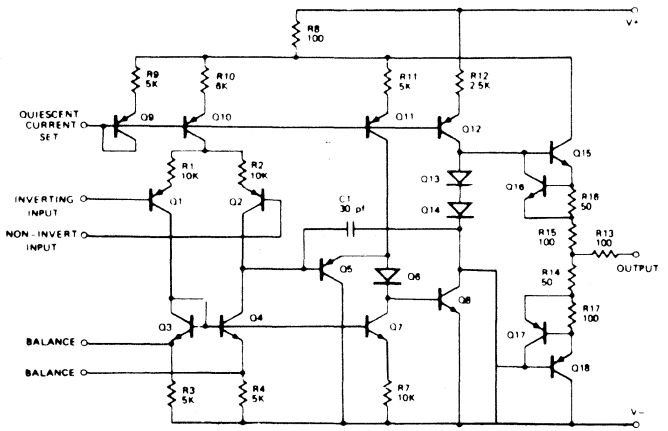
SG4250/4250C

The SG4250/4250C are intended for applications requiring extremely low internal power consumption. The device is pin compatible with the 741 type operational amplifiers and is an exact replacement for the industry standard 4250/4250C.

FEATURES

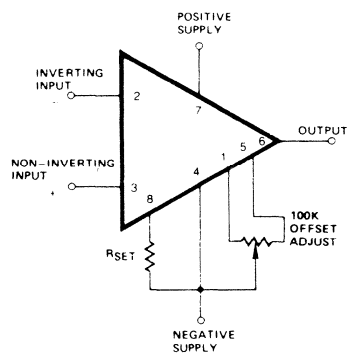
- **± 1V to ± 18V power supply operation**
- **W standby power consumption**
- **5nA input bias current**
- **35nV √Hz input noise voltage (typ)**
- **Internally compensated**

SCHEMATIC DIAGRAM (Each Amplifier)



NOTE: Balance adjust not available in triple op amp.

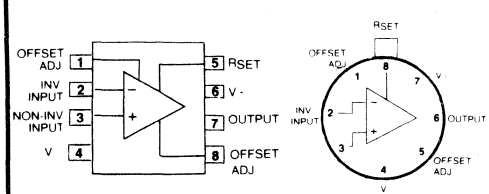
CONNECTION DIAGRAM



NOTE: T_{SET} is required to establish the internal operating currents. Its value may be determined on the table given on page 2.

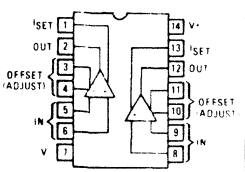
CONNECTION DIAGRAMS (Top Views)

SINGLE



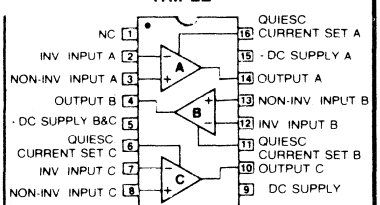
TOP VIEW
1250/2250/3250/4250/4250C

DUAL



TOP VIEW
1252/2252/3252

TRIPLE



TOP VIEW
1253/2253/3253

SG1250/SG2250/SG3250 — Single
SG1252/SG2252/SG3252 — Dual
SG1253/SG2253/SG3253 — Triple
SG4250/SG4250C — Single

ADVANCED DATA

Performance data described herein represent design goals. Final device specifications are subject to change.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage (Note 1)	±15V
Common Mode Input Voltage (Note 2)	±15V
Output Short Circuit Duration	Indefinite (Note 3)
Power Dissipation (Pkg. Limitation)	
T-Package	680mW
Derate above 25°C	5.4mW/°C
M-Package	400mW
Derate above 25°C	4.0mW/°C
Storage Temperature Range	
T,Y Package	−65°C to +150°C
M-Package	−55°C to +125°C

Note 1. This rating applies to maximum voltage differential between input terminals. The maximum input voltage on either input terminal is limited to supply voltage up to a limit of ±15V.

Note 2. This rating limited to ±supply voltage to a maximum of ±15V.

Note 3. With the output shorted to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

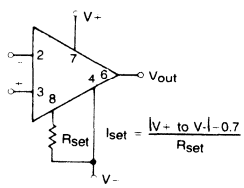
SETTING QUIESCENT CURRENT

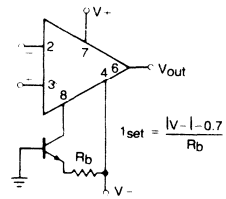
RESISTOR BIASING

Vs	QUIESCENT CURRENT 10μA	30μA	100μA	300μA
±1.5	1.5MΩ	470KΩ	150KΩ	— —
±3	3.3MΩ	1.1MΩ	330KΩ	100KΩ
±6	7.5MΩ	2.7MΩ	750KΩ	220KΩ
±9	13MΩ	4MΩ	1.3MΩ	350KΩ
±12	18MΩ	5.6MΩ	1.5MΩ	510KΩ
±15	22MΩ	7.5MΩ	2.2MΩ	620KΩ

CURRENT SOURCE BIASING

IQ	10μA	30μA	100μA	300μA
Iset	1.3μA	4μA	15μA	50μA





ELECTRICAL CHARACTERISTICS

PARAMETERS/CONDITIONS		1250/1252/1253[1]	2250/2252/2253[1]	3250/3252/3253[1]	4250[2]	4250C[2]	UNITS
Operating Temperature Range		−55 to +125	0 to +70	0 to +70	55 to +125	0 to +70	°C
Supply Voltage		±18					
Differential Input Voltage[3]		±15					
Common Mode Range[3]		±15					
Package Types		T,Y	T,Y,M	T,Y,M	T,Y	T,Y,M	
Input Offset Voltage	RS <100KΩ RS < 10KΩ	— 3(4)	— 3(4)	— 6.0(7.5)	3(4) —	— 7.5	mV
Input Bias Current	VS = ±3V VS = ±15V	18(20) 12(15)	18(20) 12(15)	40(50) 25(30)	 (15)[2]	 30(50)[2]	nA
Input Offset Current		5(8)	5(8)	10(15)	(5)	10(15)	nA
Input Resistance		3	3	3	3	3	M
Large Signal Voltage Gain	RL = 10K VS = ±3V RL = 10K VS = ±15V	40(25 400(50)	40(25) 100(50)	40(25) 75(50)	— 100(50)[2]	— 75(50)[2]	V/mV
Output Voltage Swing	VS = ±3V, RL = 10KΩ VS = ±15V, RL = 10KΩ		±1.5(±1.0) ±11(±10)		— ±11(±10)[2]	— ±11[2]	V
CMRR RS<10KΩ		(70)	(70)	(70)	(70)	(70)	dB
PSRR RS<10KΩ	VS = 3V VS = ±15V	(200) (150)	(200) (150)	(200) (150)	 (150)[2]	 (150)[2]	μV/V
Power Consumption	VS = ±3V VS = ±15V, RL = 0	(240) (1200)	(240) (1200)	(240) (1200)	 (480)[2]	 (600)[2]	μW
Average TC of Offset Voltage	RS = 10K (±15V for 1250)	4(typ)	4(typ)	6(typ)	5(typ)	5(typ)	μV/°C
Average TC of Offset Current	RS = 20K (±15V for 1250)	2(typ)	2(typ)	1(typ)	1.7(typ)	1(typ)	pA/°C
Equiv. Input Noise Voltage	f=10Hz (±15V for 1250)	35(typ)	35(typ)	35(typ)	35(typ)	35(typ)	nV/√Hz
Equiv. Input Noise Current	f=10Hz (±15V for 1250)	0.5(typ)	0.5(typ)	0.5(typ)	0.5(typ)	0.5(typ)	pA/√Hz
Slew Rate	RL = 10K, CL = 100pF	0.2(typ)	0.2(typ)	0.2(typ)	0.16(typ)	0.16(typ)	V/μS
Small Signal Unity Gain-Bandwidth	Rf = 0 Vin = 20mV, RL = 20KΩ	—	—	—	250(typ)	250(typ)	kHz

Parameters for 1250/1252/1253 are min/max limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), for supply voltage of ±3V to ±15V and for a quiescent current of 30 A established by an R_{set} of 1.1.

Parameters for 4250/4250C are min/max limits either at T 25°C (for over operating temperature range if enclosed in parentheses.) for supply voltage of -6 and quiescent current of 30.

SG1536/1436/1436C

SG1536/1436/1436C are intended specifically for use in high voltage applications where high common mode input ranges, high output voltage swings and low input currents are required. These devices are internally compensated and are pin compatible with industry-standard operational amplifiers.

- Usable with up to ±40V supplies
- Provides up to ±30V output voltage swing
- Common mode voltages to ±24V
- Input current 35nA max over temperature

SG1556/1456/1456C

This series offers excellent input characteristics plus a five-times improvement in slew rate over conventional amplifiers.

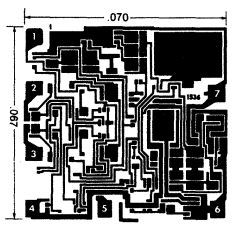
- Low bias current 15nA max
- Low input offset voltage 4.0mV max
- Fast slew rate 2.5V/μs typical
- Low power consumption 45mW max
- Output short circuit protection

PARAMETERS*	1536[1]	1436[1]	1436C[1]	1556	1456	1456C	UNITS
Supply Voltage	±40	±34	±30	±15	±15	±15	V
Operating Temperature Range	−55 to +125	0 to +75	0 to +75	−55 to +125	0 to +75	0 to +75	°C
Package Types	T, Y			T, Y			—
Input Offset Voltage	5.0 (7.0)	10	12	4.0 (6.0)	10 (14)	12	mV
Input Offset Current	3.0 (7.0)	10 (14)	25	2.0 (5.0)	10 (14)	30	nA
Input Bias Current	20 (35)	40 (55)	90	15 (30)	30 (40)	90	nA
Large Signal Voltage Gain	100 (50)	70 (50)	50	100 (40)	70 (40)	25[3]	V/mV
Common Mode Rejection	80	70	50	80	70	110 (typ)	dB
Power Supply Rejection	100	200	50	100	200	75 (typ)	μV/V
Input Common Mode Range[2]	±24	±22	±18	±12	±11	±10.5	V
Differential Input Voltage (V)	±(V+ + |V−| − 3V)			$\pm V_S$	$\pm V_S$	$\pm V_S$	V
Unity Gain Bandwidth	1.0 (typ)	1.0 (typ)	1.0 (typ)	1.0 (typ)	1.0 (typ)	1.0 (typ)	MHz
Slew Rate[4]	2.0 (typ)	2.0 (typ)	2.0 (typ)	2.5 (typ)	2.5 (typ)	2.5 (typ)	V/μS
Supply Current	4.0	5.0	5.0	1.5	3.0	4.0	mA
Output Voltage Swing R_L = 2kΩ	±22[1]	±20[1]	±20[1]	±12	±11	±10	V
R_L = 10kΩ	±30[5]	—	—	—	—	—	V
Noise (typ) A_V = 100, R_S = 10kΩ, f = 1.0 KHz, BW = 1.0Hz	50	50	50	45	45	45	nV/(Hz)½ (typ)

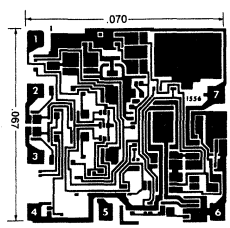
*Parameters apply over supply voltage range and are min./max. limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

[1] V_S = ±28V [2] V_S = ±15V [3] Inputs are shunted with back-to-back diodes for over voltage protection

[4] R_L = 5 kΩ [5] R_L = 5.0kΩ, V_S = ±36V.

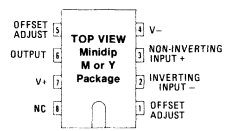


SG1536/1436/1436C Chip (See T-package diagram for pad functions)

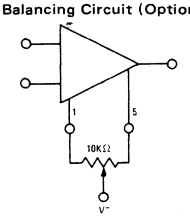


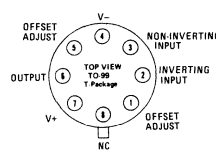
SG1556/1456/1456C Chip
(See T-package diagram for pad functions)

CONNECTION DIAGRAMS



Balancing Circuit (Optional)





SG1660

The SG1660 is a superior, functional, and pin for pin, replacement for the 301A, 748C and 201 operational amplifiers. The SG1660 is also frequently a desirable replacement for the 308/308A types due to its lower cost.

- 15nA input bias current
- 2.0nA input offset current
- Low power – 7.5mW (typ)
- CMRR of 80dB
- PSRR of 80dB
- Available in minidip

SG1760

The SG1760 is an internally compensated version of the SG1660 and is a superior replacement for the 307 and 741 type op amps.

- 15 nA input bias current
- 2.0 nA input offset current
- Low power – 7.5 mW (typ)
- CMRR of 80 dB
- PSRR of 80 dB
- Available in minidip

2

PARAMETERS*	1660	1760	UNITS
Supply Voltage	±5 to ±15	±5 to ±15	V
Operating Temperature Range	0 to +70	0 to +70	°C
Package Types	T, J, M, Y, F		–
Input Offset Voltage	7.5 (10.0)	7.5 (10.0)	mV
Input Offset Current	2.0 (4)	2.0 (4)	nA
Input Bias Current	15 (25)	15 (25)	nA
Temp Coeff. Input Offset Voltage	30	30	μV/°C
Temp Coeff. Input Offset Current	0.04	0.04	nV/°C
Large Signal Voltage Gain	25 (15)[1]	25 (15)[1]	V/mV
Common Mode Rejection	(80)	(80)	dB
Power Supply Rejection	(80)	(80)	μV/V
Input Common Mode Voltage Range[3]	(±13.5)[3]	(±13.5)[3]	V
Differential Input Voltage	±1[4]	±1[4]	V
Slew Rate A_V = 1,	0.1	0.1	V/μS
Slew Rate A_V = 10	1 (typ)	1 (typ)	V/μS
Unity Gain Bandwidth	0.3 (typ)	0.3 (typ)	MHz
Supply Current	0.75[2]	0.75[2]	mA
V_{out} R_L = 10kΩ	±13	±13	V
Noise			
R_S = 1kΩ f = 10Hz to 10kHz	4	4	μV(rms)
R_S = 500kΩ f = 10Hz to 10kHz	20	20	(typ)

*Parameters apply over supply voltage range and are min./max. limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

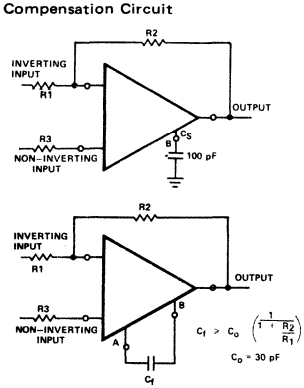
[1] R_L = 10kΩ, V_S = ±15V, V_{out} = ±10V

[2] T_A = 70°C (1000 μA at 0°C)

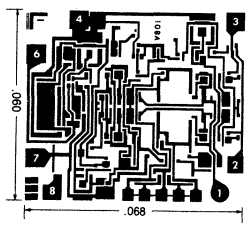
[3] V_S = ±15V

[4] Inputs are shunted with back-to-back diodes for overvoltage protection.

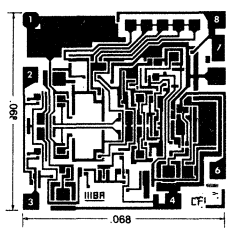
Compensation Circuit



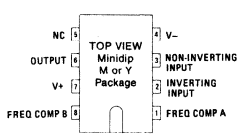
(not required for 1760)

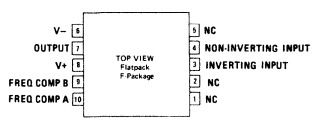


SG1660 Chip (See T-package diagram for pad functions)

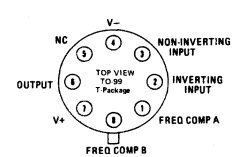


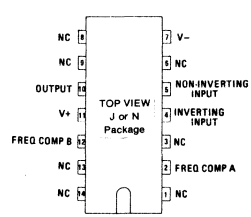
SG1760 Chip (See T-package diagram for pad functions)





CONNECTION DIAGRAMS





Quad High-Performance Operational Amplifiers

SG4136 / SG4136C

DESCRIPTION

The SG4136 and SG4136C are quad high-performance operational amplifiers with each amplifier electrically similar to uA741 except that offset null capability is not provided.

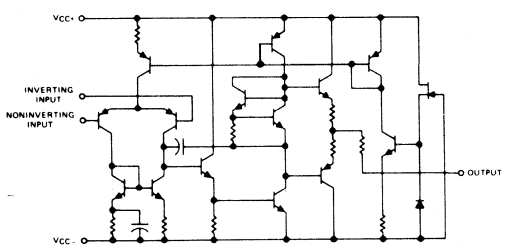
The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The SG4136 is characterized for operation over the full military range of −55°C to 125°C; the SG4136C is characterized for operation from 0°C to 70°C.

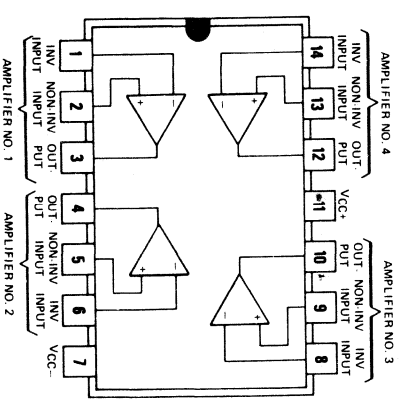
FEATURES

- **Continuous Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-up**
- **Unity Gain Bandwidth 3 MHz Typical**
- **Gain and Phase Match Between Amplifiers**
- **Designed to be Interchangeable with Raytheon RM4136 and RC4136**

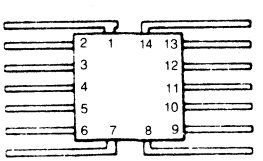
SCHEMATIC (each amplifier)



CONNECTION DIAGRAM

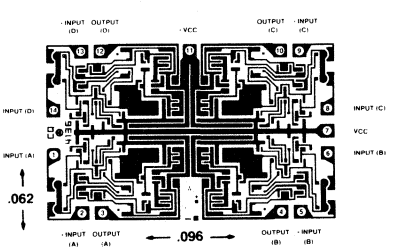


J/N PKG



F PKG

PIN	FUNCTION	PIN	FUNCTION
1	−INPUT (A)	8	−INPUT C
2	+INPUT (A)	9	+INPUT (C)
3	OUTPUT (A)	10	OUTPUT (C)
4	OUTPUT (B)	11	+VCC
5	+INPUT (B)	12	OUTPUT (D)
6	−INPUT (B)	13	+INPUT (D)
7	−VCC	14	−INPUT (D)



CHIP LAYOUT

SG4136 / SG4136C

ABSOLUTE MAXIMUM RATINGS

	SG4136	SG4136C	UNIT
Supply voltage V_{CC+} (See note 1)	22	18	V
Supply voltage V_{CC-} (see Note 1)	−22	−18	V
Differential input voltage (see Note 2)	±30	±30	V
Input voltage (any input, see Notes 1 and 3)	±15	±15	V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	800	800	mW
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		SG4136 MIN	SG4136 TYP	SG4136 MAX	SG4136C MIN	SG4136C TYP	SG4136C MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		0.5	5		0.5	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current		25°C		5	200		5	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		40	500		40	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±14		±12	±14		V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		R_L = 2 kΩ	25°C	20	26		20	26		
		$R_L \geq$ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±10 V	25°C	50	350		20	300		V/mV
			Full range	25			15			
B_1	Unity-gain bandwidth		25°C	2	3.5			3		MHz
r_i	Input resistance		25°C	0.3	5		0.3	5		MΩ
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	70	90		70	90		dB
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	$R_S \leq 10$ kΩ	25°C		30	150		30	150	μV/V
V_n	Equivalent input noise voltage (close-loop)	A_{VD} = 100, R_S = 1 kΩ, f = 1 kHz, BW = 1 Hz	25°C		10			10		nV/√Hz
I_{CC}	Supply current (All four amplifiers)	No load, No signal	25°C		5	11.3		5	11.3	mA
			MIN T_A		6	13.3		6	13.7	
			MAX T_A		4.5	10		4.5	10	
P_D	Total power dissipation (All four amplifiers)	No load, No signal	25 C		150	340		150	340	mW
			MIN T_A		180	400		180	400	
			MAX T_A		135	300		135	300	
V_{o1}/V_{o2}	Channel separation (Open loop, A_{VD} = 100)	R_S = 1 kΩ, f = 10 kHz	25°C		105			105		dB
			25°C		105			105		

† All characteristics are specified under open-loop operation, unless otherwise noted. Full range for SG4136 is −55°C to 125°C and for SG4136C is 0°C to 70°C.

OPERATING CHARACTERISTICS, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SG4136 MIN	SG4136 TYP	SG4136 MAX	SG4136C MIN	SG4136C TYP	SG4136C MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF		0.13			0.13		μs
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF		1.5			1.0		V/μs

INTERFACE CIRCUITS

Line Drivers
Line Receivers
Quad Line Receivers
Quad Bus Receivers
Quad Bus Tranceivers
Voltage Comparators
Quad Comparators
Dual Peripheral Drivers
Power Switch Drivers
Memory Drivers
Dual Sense/Data Register

SG111/211/311

The SG111/211/311 are medium speed, high input impedance devices which are especially well suited for use in level detection and low level voltage sensing applications. Operation may be obtained from supply voltages ranging from ±15V down to a single +5V source.

The output, an open collector NPN capable of switching 50V and 50mA, can drive RTL, DTL, TTL, MOS logic, relays or lamps. Both input and output can be isolated from ground and the output can drive loads referred to a positive supply, ground or a negative supply. These devices also offer offset balance, strobe capability and pin configuration of the SG710 Comparator.

- **Differential input voltage range of ±30V**
- **150nA maximum bias current**
- **Consumes 135mW at ±15V**

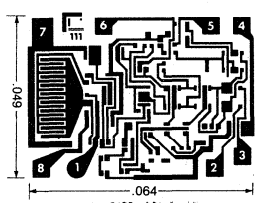
PARAMETERS*	111	211	311	UNITS
Operating Temperature Range	−55 to +125	−25 to +85	0 to +70	°C
Package Types	T,J	T, J, M		
Supply Voltage	±15			V
Input Offset Voltage $R_S \leq 50k$	3 (4.0)[2]		7.5 (10.0)[2]	mV
Input Offset Current	10 (20)[2]		50 (70)[2]	nA
Input Bias Current	100 (150)		250 (300)	nA
Voltage Gain	200 (typ)		200 (typ)	V/mV
Response Time[1]	200 (typ)		200 (typ)	nS
Saturation Voltage I_{sink} = 50 mA	1.5		1.5	V
V^+ = 4.5V, V^- = 0V, I_{sink} = 8 mA	0.4		0.4	V
Output Leakage Current	10 (500)		50	nA
Differential Input Voltage max	±30		±30	V
Total Supply Voltage, V_{84} max	36		36	V
Input Voltage Range	±14 (typ)		±14 (typ)	V
Positive Supply Current	6.0		7.5	mA
Negative Supply Current	5.0		5.0	mA
Output Voltage, V_{74}	50[3]		40[3]	V

*Parameters apply over supply voltage range and are min./max. limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

[1] The response time specified is for a 100mV input step with 5mV overdrive.

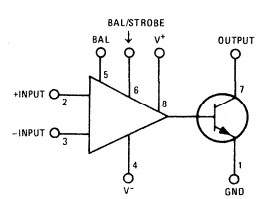
[2] The offset voltages and offset currents given are the maximum values required to drive the output down to 1V or up to 14V with 1mA load.

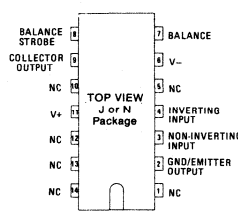
[3] Output voltage levels can be changed for compatibility with DTL and T2L logic levels.

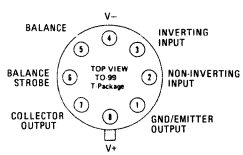


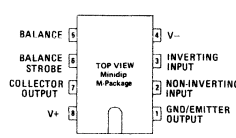
SG111/211/311 Chip (See T-package diagram for pad functions)

CONNECTION DIAGRAMS









SG139/239/339 SG139A/239A/339A / SG3302* SG139B / 239B / 339B

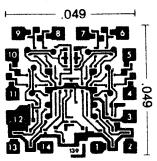
The SG139 series describes a monolithic IC containing four independent voltage comparators designed to provide maximum utility and versatility in a single package. Unique features of this device include the ability to operate with either a single or dual-polarity power supply and a common-mode voltage range including ground, even when using a single supply voltage. Additionally, the open-collector output stage provides easy interfacing with all types of logic circuitry.

- **Wide supply voltage range: 2 to 36 volts or ±1 to ±18 volts.**
- **Low supply current (0.8 mA) insensitive to supply voltage.**
- **Input bias current of 25 nA typically.**
- **Compare voltages at ground common mode.**
- **Output compatible with DTL, TTL, ECL, MOS, and CMOS Logic.**

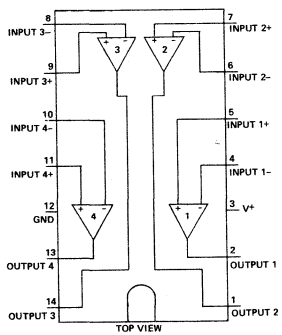
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+36V or ±18V
Differential Input Voltage	36V
Input Voltage Range (Note 1)	-0.3V to +36V
Input Current (V_{IN} <-0.3Vdc)	50mA
Output Sink Current	20mA
Power Dissipation	
N Package (plastic)	600mW
Derate above 25°C	6.0mW/°C
J Package (cerdip)	1000mW
Derate above 25°C	6.7mW/°C
Output Short Circuit to Gnd (Note 2)	Continuous
Operating Temperature Range	
SG139 (J-pkg only)	-55°C to +125°C
SG239	-25°C to +85°C
SG339	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

CONNECTION DIAGRAM



CHIP BONDING DIAGRAM



ELECTRICAL CHARACTERISTICS (T_A = 25°C, see Note 3)

Parameter	Conditions	SG139 SG139A/139B Min.	Typ.	Max.	SG239/339 SG239A/339A SG239B/339B Min.	Typ.	Max.	Units
Input Offset Voltage	At Output Switch Point, $V_O \cong$ 1.4 V_{DC}, V_{REF} = +1.4 V_{DC} and R_S = 0Ω		±2.0	±5.0		±2.0	±5.0	mV_{DC}
*"A" Versions				±2.0			±2.0	mV_{DC}
Input Bias Current (Note 4)	$I_{IN(+)}$ or $I_{IN(-)}$ With Output in Linear Range		25	100		25	250	nA_{DC}
"B" Versions (only)				200			500	
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$		±3	±25		±5	±50	nA_{DC}
"B" Versions (only)				±50			±100	
Input Common-Mode Voltage Range (Note 1)		0		V^+-1.5	0		V^+-1.5	V_{DC}
Supply Current	R_L = ∞ On All Comparators		0.8	2.0		0.8	2.0	mA_{DC}
"B" Versions (only)				3.0			3.0	
Voltage Gain	$R_L \geq$ 15kΩ		200			200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = +1.4 V_{DC}, V_{RL} = 5.0 V_{DC} and R_L = 5.1kΩ		300			300		ns
Response Time (Note 5)	V_{RL} = 5.0 V_{DC} and R_L = 5.1 kΩ		1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geq$ + 1.0V_{DC}, $V_{IN(+)}$ = 0	6		16	6	16		mA_{DC}
"B" Versions (only)	and $V_O \leq$ + 1.5 V_{DC}	15		25	15	25		
Saturation Voltage	$V_{IN(-)} \geq$ + 1.0 V_{DC}, $V_{IN(+)}$ = 0 and $I_{SINK} \leq$ 4.0 mA		250	500		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq$ + 1.0 V_{DC}, $V_{IN(-)}$ = 0 and V_{OUT} = 5.0 V_{DC}		0.1			0.1		nA_{DC}
T_A = Operating Temperature Range								
Input Offset Voltage	At Output Switch Point, $V_O \cong$ 1.4 V_{DC}, V_{REF} = +1.4 V_{DC} and R_S = 0Ω			±9.0			±9.0	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150	nA_{DC}
"B" Versions (only)				±200			±300	
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ With Output in Linear Range			300			400	nA_{DC}
"B" Versions (only)				500			800	
Input Common-Mode Voltage Range		0		V^+-2.0	0		V^+-2.0	V_{DC}
Saturation Voltage	$V_{IN(-)} \geq$ + 1.0 V_{DC}, $V_{IN(+)}$ = 0 and $I_{SINK} \leq$ 4.0 mA			700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq$ + 1.0 V_{DC}, $V_{IN(-)}$ = 0 and V_{OUT} = 30 V_{DC}			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep All V_{IN}'s ≥ 0 V_{DC} (or V⁻, if used)			36			36	V_{DC}

Note 1: If either input of any comparator goes more than 0.3 volt below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This condition is not destructive providing the input current is limited to less than 50 mA.
Note 2: Short circuits from the output to V+ can cause excessive heating and eventual destruction.
Note 3: Unless otherwise stated, these specifications apply for V^+ = 5 volts for the SG139, 239 and 339; and V^+ = 15 volts for the SG139A, 239A, and 339A.
Note 4: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
Note 5: The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger overdrive signals 300 ns can be obtained.

* Contact factory for 3302 test limits.

APPLICATIONS INFORMATION

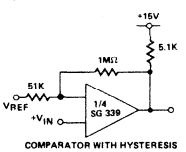
These comparators are high gain, wide bandwidth devices; which, like most circuits of this type, can easily oscillate with stray feedback paths from output to input. This only occurs during the output voltage transition intervals as the comparator changes state and can be minimized by reducing the value of the input resistors to less than 10kΩ, using P.C. board wiring rather than sockets, or providing a small amount of positive feedback to cause rapid transitions. Power supply bypassing is not normally required with this circuit.

All pins of any unused comparators should be grounded.

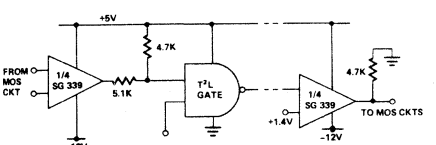
The differential input voltage may be larger than V+ without causing damage but if negative excursions greater than -0.3 volt are possible, protection should be provided by a clamp diode and/or input resistor.

The output of this comparator is an uncommitted collector of a grounded-emitter NPN transistor. Several collectors may be tied together to provide a wired-OR function. An output pull-up resistor can be connected to any available power supply voltage up to 36 volts with respect to the GND terminal, regardless of the voltage level applied to the V+ terminal. The output can also be used as a simple SPST switch to ground when no pull-up resistor is used.

The amount of current which the output transistor can sink is limited by its drive to about 16 mA. Exceeding this current will cause the transistor to come out of saturation and the output voltage will rise very rapidly. The amount of saturation voltage is determined by the r_{sat} of the output transistor which is approximately 60 ohms.



COMPARATOR WITH HYSTERESIS



MOS TO TTL TO MOS LEVEL SHIFT

SG710/710C

The SG710/710C are high-speed voltage comparators designed for use in level detection, low-level sensing and memory applications. Inherent component matching provides low offset voltage and drift as well as high accuracy and fast response. The output of the comparator is compatible with all forms of saturating logic.

SG711/711C

The SG711/SG711C are dual voltage comparators designed for use in core-memory sense amplifier applications, pulse height detectors, and as a double-ended limit sensor for automatic go/no-go test equipment. Inherent component matching provides low offset voltage and drift as well as high accuracy and fast response. With an output compatible with all forms of saturation logic, the device also has provisions for independent strobing of each comparator channel.

PARAMETERS*	710	710C	711[3]	711C[3]	UNITS
Operating Temperature Range	−55 to +125	0 to +70	−55 to +125	0 to +70	°C
Package Types	T, J, N		T, J, N		—
Supply Voltage (max)	+14.0, −7.0	+14.0, −7.0	+14.0, −7.0	+14.0, −7.0	V
Input Offset Voltage[2]	2.0 (3.0)	5.0 (6.5)	3.5 (6.0)	5.0 (10)	mV
Input Offset Current[2]	3.0 (7.0)	5.0 (7.5)	10 (20)	15 (25)	μA
Input Bias Current	20 (45)	25 (40)	75 (150)	100 (150)	μA
Voltage Gain	1250 (1000)	1000 (800)	750 (500)	700 (500)	V/V
Response Time[1] (typ)	40 (typ)	40 (typ)	60 (max)	40 (typ)	nS
Differential Input Voltage	±5.0	±5.0	±5.0	±5.0	V
Output Sink Current	2.0 (0.5)	1.6 (0.5)	0.5	0.5	mA
Positive Output Voltage	2.5/4.0	2.5/4.0	2.5/5.0	2.5/5.0	V
Negative Output Voltage	−1.0/0	−1.0/0	−1.0/0	−1.0/0	V
Input Common Mode Range	±5.0	±5.0	±5.0	±5.0	V
Common Mode Rejection Ratio	80	70	—	—	dB
Power Supply Current	9.0	9.0	10.0	7.2 (typ)	mA
Power Consumption	150	150	150	150	mW
Strobe Current	—	—	2.5	2.5	mA

*Parameters apply over supply voltage range and are min./max. limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

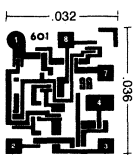
[1] The response time specified is for a 100mV input step with 5mV overdrive.

[2] The offset voltages and offset currents given are the maximum values required to drive the output to 1.4Vdc at 25°C, 1.8Vdc at 0° or −55°C, 1.0Vdc at +70° or 125°C.

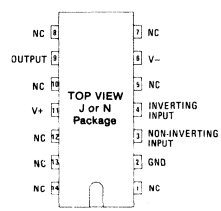
[3] Each comparator.

CONNECTION DIAGRAMS

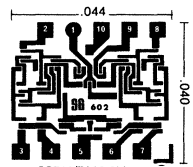
SG710/710C



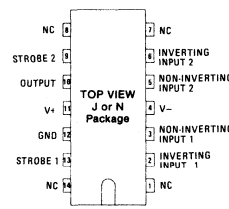
SG710/710C Chip
(See T-package diagram for pad functions)

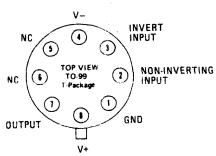


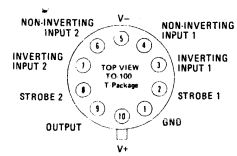
SG711/711C



SG711/711C Chip
(See T-package diagram for pad functions)







SG1488

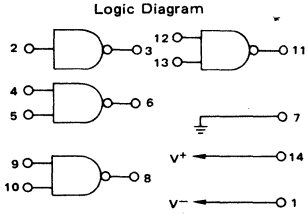
The SG1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

- **Current limited output 10mA typ**
- **Power-Off source impedance 300 ohms minimum**
- **Simple slew rate control with external capacitor**
- **Flexible operating supply range**
- **Compatible with all DTL and TTL logic families**

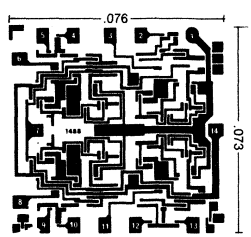
PARAMETERS*	1488	UNITS
Supply Voltage (max, T_A = 25°C)	+15, −15	V
Input Signal Voltage (max, T_A = 25°C)	$-15 \leq V_{in} \leq 7.0$	V
Output Signal Voltage (max, T_A = 25°C)	±15	V
Package Types	J	–
Operating Temperature Range	0 to +75	°C
Forward Input Current (V_{in} = 0 Vdc)	1.6	mA
Reverse Input Current (V_{in} = +5.0 Vdc)	10	μA
Output Voltage High		
(V_{in} = 0.8 Vdc, R_L = 3.0kΩ, V^+ = +9.0 Vdc, V^- = −9.0 Vdc)	+6.0	V
(V_{in} = 0.8 Vdc, R_L = 3.0kΩ, V^+ = +13.2 Vdc, V^- = −13.2 Vdc)	+9.0	
Output Voltage Low		
(V_{in} = 1.9 Vdc, R_L = 3.0kΩ, V^+ = +9.0 Vdc, V^- = −9.0 Vdc)	−6.0	V
(V_{in} = 1.9 Vdc, R_L = 3.0kΩ, V^+ = +13.2 Vdc, V^- = −13.2 Vdc)	−9.0	
Positive Output Short-Circuit Current	+6.0/+12	mA
Negative Output Short-Circuit Current	−6.0/−12	mA
Output Resistance ($V^+ = V^- = 0$, $\lvert V_o \rvert$ = ±2.0V)	300 (min)	Ω
Positive Supply Current (R_L = ∞)		
V_{in} = 0.8/1.9V V^+ = +9V	6/20	mA
V^+ = 12V	7/25	
V^+ = 15V	12/34	
Negative Supply Current (R_L = ∞)		
V_{in} = 0.8/1.9V V^- = −9V	0/−17	mA
V^- = −12V	0/−23	
V^- = −15V	−2.5/−34	
Power Dissipation		
(V^+ = 9.0 Vdc, V^- = −9.0 Vdc)	333	mW
(V^+ = 12 Vdc, V^- = −12 Vdc)	576	
SWITCHING CHARACTERISTICS (V^+ = +9.0 ± 1% Vdc, V^- = −9.0 ± 1% Vdc, T_A = +25°C)		
Propagation Delay Time (Z_L = 3.0k and 15 pF)	200	nS
Fall Time (Z_L = 3.0k and 15 pF)	75	nS
Propagation Delay Time (Z_L = 3.0k and 15 pF)	120	nS
Rise Time (Z_L = 3.0k and 15 pF)	100	nS

*Parameters are min/max limits with V^+ = +9.0 ± 1% Vdc, V^- = −9.0 ± 1% Vdc, T_A = 0 to +75°C unless otherwise noted.

Logic Diagram

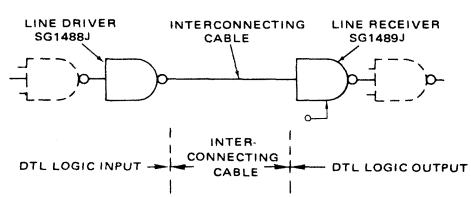


CONNECTION DIAGRAM FOR J-PACKAGE



SG1488 Chip (See logic diagram for pad functions)

Typical Application



SG1489/1489A

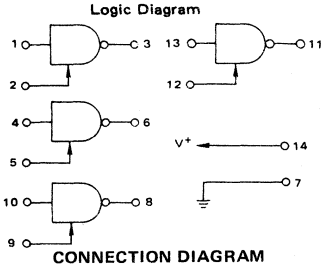
The SG1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

- **Input Resistance – 3.0k to 7.0kΩ**
- **Input Signal Range – ±30 Volts**
- **Input Threshold Hysteresis Built In**
- **Response Control**
  - **a) Logic Threshold Shifting**
  - **b) Input Noise Filtering**

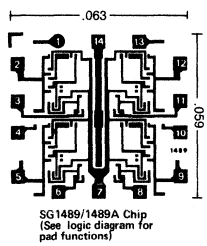
PARAMETERS*		1489/1489A	UNITS
Power Supply Voltage (max, T_A = 25°C)		10	V
Input Signal Range (max, T_A = 25°C)		±30	V
Output Load Current (T_A = 25°C)		20	mA
Package Types		J	–
Power Dissipation (Package Limitation, Ceramic Dual In-Line Package)		1000	mW
Derate above T_A = +25°C		6.7	mW/°C
Operating Temperature Range		0 to +75	°C
Storage Temperature Range		–65 to +175	°C
Positive Input Current	(V_{in} = +25 Vdc)	3.6/8.3	mA
	(V_{in} = +3.0 Vdc)	0.43	
Negative Input Current	(V_{in} = –25 Vdc)	–3.6/–8.3	mA
	(V_{in} = –3.0 Vdc)	–0.43	
Input Turn-On Threshold Voltage (T_A = +25°C, $V_{OL} \leq$ 0.45V)	SG1489J	1.0/1.5	V
	SG1489AJ	1.75/2.25	
Input Turn-Off Threshold Voltage (T_A = +25°C, $V_{OH} \geq$ 2.5V, I_L = –0.5 mA)	SG1489J	0.75/1.25	V
	SG1489AJ	0.75/1.25	
Output Voltage High	(V_{in} = 0.75V, I_L = –0.5mA)	2.6/5.0	V
	(Input Open Circuit, I_L = –0.5 mA)	2.6/5.0	
Output Voltage Low	(V_{in} = 3.0V, I_L = 10mA)	0.45	V
Power Supply Current	(V_{in} = +5.0Vdc)	26	mA
Power Consumption	(V_{in} = +5.0Vdc)	130	mW
SWITCHING CHARACTERISTICS (T_A = +25°C)			
Propagation Delay Time	(R_L = 3.9kΩ)	85	nS
Rise Time	(R_L = 3.9kΩ)	175	nS
Propagation Delay Time	(R_L = 390 Ω)	50	nS
Fall Time	(R_L = 390 Ω)	20	nS

*Parameters are min./max. limits with response control pin open, V^+ = +5.0 Vdc ±1%, T_A = 0 to +75°C unless otherwise noted.

Logic Diagram

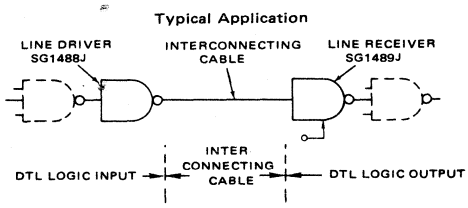


CONNECTION DIAGRAM FOR J-PACKAGE



SG1489/1489A Chip (See logic diagram for pad functions)

Typical Application



SG1627 / 3627

DESCRIPTION

The SG1627 and SG3627 devices are monolithic, high-speed driver integrated circuits designed to interface digital control logic with high current loads. Each device contains two independent drivers which will either source or sink up to 500 mA of current. The sink transistor is designed as a saturating switch while the source transistor can be used either as a switch or as a constant current generator with external resistor programming.

Each half of this device contains both inverting and non-inverting inputs which have two volt thresholds for high noise immunity. Either input can be used alone to switch the output, or one input can be strobed with the other. These units have been designed to directy interface with the SG1524 Regulating Pulse Width Modulator Circuit.

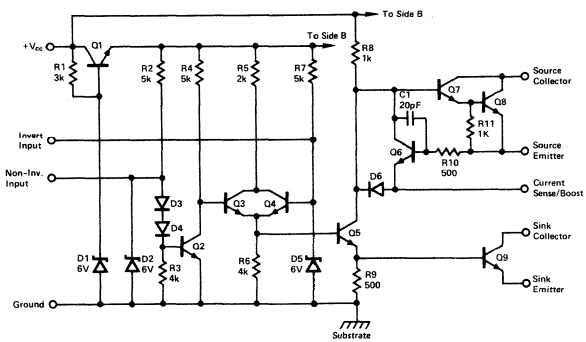
These devices are supplied in ceramic 16-pin D.I.L. packages. The SG1627 is specified for operation over a -55°C to +125°C temperature range while the SG3627 is intended for industrial applications of 0°C to +100°C.

FEATURES

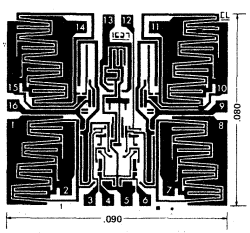
- **Two independent driver circuits**
- **Outputs will source or sink currents to 500 mA**
- **100 nSec response time**
- **Full compatibility with SG1524 PWM circuit**
- **Constant current drive capability**
- **Two volt threshold for high noise immunity**
- **Source and sink can be separated for complementary outputs**

3

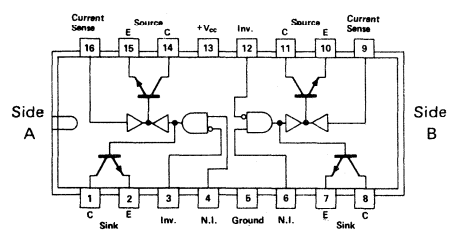
SCHEMATIC (one half of total device shown)



CHIP LAYOUT



CONNECTION DIAGRAM (TO–116 OUTLINE)



SG1627 / 3627

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	30V
Output Collector Voltage	30V
Source or Sink Current	500 mA
Input Voltage	5.5V
Input Current	10 mA
Avg. Total Power Dissipation (Note 1)	1000 mW
Derate Above 50°C	10 mW/°C

Operating Temperature Range	
SG1627	-55°C to +125°C
SG3627	0°C to +100°C
Storage Temperature Range	-65°C to +150°C

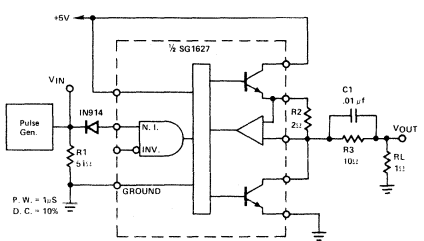
Note 1: Total power dissipation is the sum of the control logic power plus the power of each source and sink output transistor, factored for duty cycle.

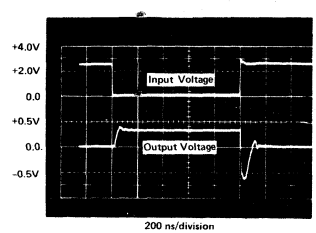
ELECTRICAL CHARACTERISITICS

Unless otherwise stated, these specifications apply for T_J = -55°C to +125°C for the SG1627 and 0°C to +100°C for the SG3627. V_{CC} = 5V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Level Input Voltage		2.8	–	5.5	Volts
Low-Level Input Voltage		0	–	1.4	Volts
Input Threshold		–	2.0	–	Volts
Low-Level Input Current	V_I = 0	–	-1.0	-2.0	mA
Source Off, Leakage Current	Collector V = 30V	–	0.3	1.0	mA
Source On, Collector Sat.	I_{source} = 50 mA	–	1.1	1.7	Volts
(Source Emitter Grounded,	I_{source} = 300 mA	–	1.2	1.9	Volts
R_{SC} = 0)	I_{source} = 500 mA	–	1.3	2.0	Volts
Source On, Emitter Voltage	I_{source} = -50 mA	(V_{CC}–3V)	–	–	Volts
Sink Off, Leakage Current	Collector V = 30V	–	1.0	100	μA
Sink On, Collector Sat.	I_{sink} = 50 mA	–	0.2	0.4	Volts
	I_{sink} = 300 mA, V_{CC} = 20V		0.5	0.7	Volts
	I_{sink} = 500 mA, I_{boost} = 25 mA		0.5	0.7	Volts
Current Limit Sense Voltage	R_{SC} = 10Ω, T_A = 25°C	600	700	800	mV
Sense Voltage Temp. Coef.	R_{SC} = 10Ω	–	1.8	–	mV/°C
Supply Current	V_{CC} = 5V		15	20	mA
(Both sink transistors on)	V_{CC} = 20V		50	65	mA
	V_{CC} = 30V		80	90	mA
Output Response, Turn On	Fig. 4, R_L = 24Ω, T_A = 25°C	–	50	–	nS
Output Response, Turn Off	Fig. 4, R_L = 24Ω, T_A = 25°C	–	100	–	nS
Thermal Resistance θ_{JA}		–	80	110	°C/W
Thermal Resistance θ_{JC}		–	45	60	°C/W

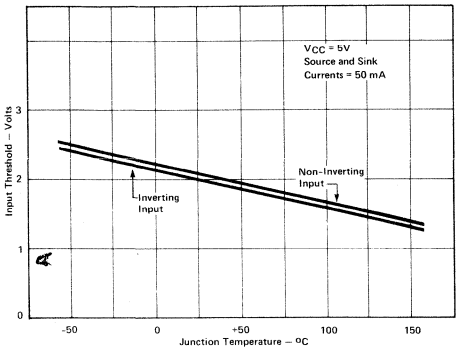
TOTEM POLE OUTPUT SWITCH CIRCUIT



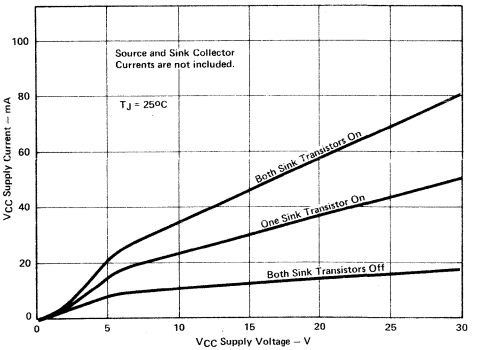


SG1627 / 3627

INPUT THRESHOLD vs. TEMPERATURE

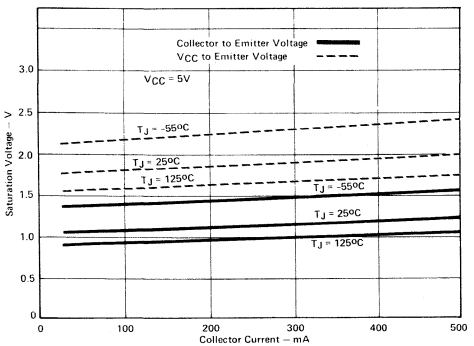


V_{CC} SUPPLY CURRENT vs. VOLTAGE

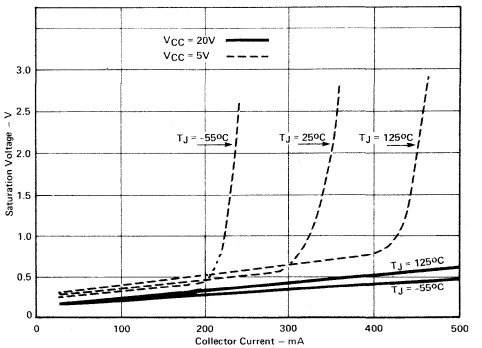


3

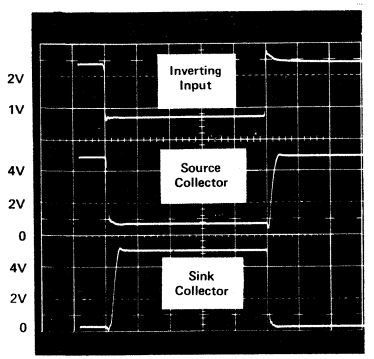
SOURCE TRANSISTOR SATURATION



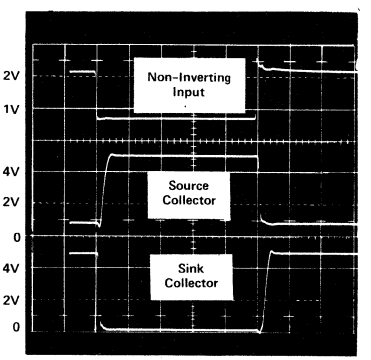
SINK TRANSISTOR SATURATION



DYNAMIC RESPONSE (See Figure 4 for Test Circuit, R_L = 24Ω)



200 ns/division



200 ns/division

SG1627 / 3627

APPLICATIONS

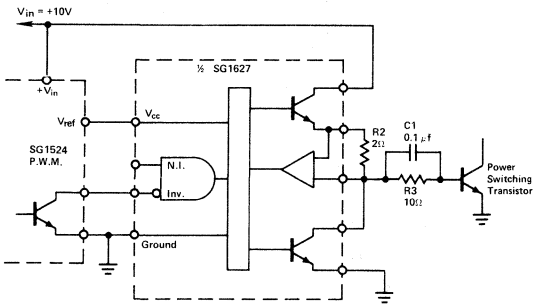


Figure 1. Basic 300 mA switched drive circuit. If the external output transistor is to be on when the driving transistor is on, use the inverting input with the non-inverting input left open. For opposite phasing, use the non-inverting input with the inverting input grounded.

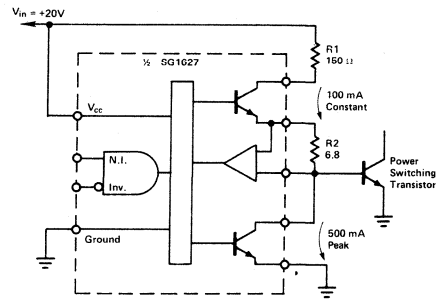


Figure 2. Use of higher input voltage provides greater drive for higher sink-transistor peak current while R2 provides constant source current. R1 helps minimize power in the SG1627. Although the sink emitter may be connected to a different ground point from pin 5, any voltage differences between them will directly affect the input threshold level.

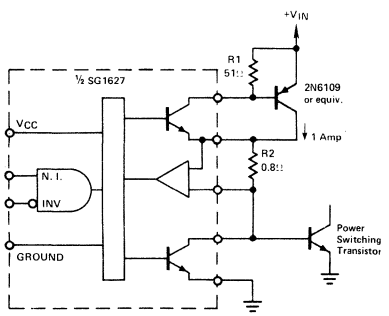


Figure 3. Additional source current or power handling capability may be added with the use of an external PNP transistor. For optimum performance, a low storage-time unit should be selected. If current limiting is not required, an NPN emitter follower could also be used for source boost.

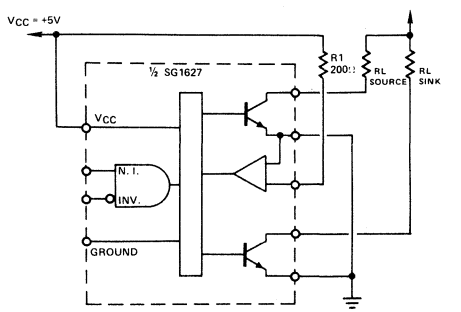


Figure 4. Source and sink transistors can be used separately for complementary outputs. At low supply voltages the sink current is limited to approximately 100 mA, but if current limiting is not required a sink drive boost may be added with R1. The current in R1 should be .05 times the sink load current to insure saturation.

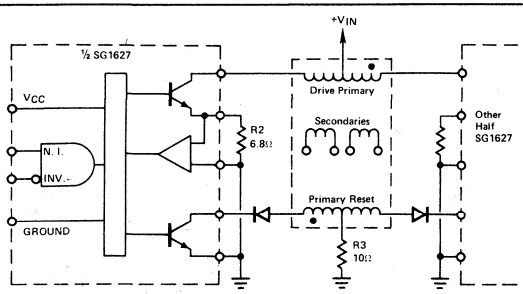


Figure 5. Source and sink transistors can be used separately for an efficient transformer driver. Here the source provides constant current drive with magnetic reset accomplished by a flux clamp utilizing the sink transistor. With the source current sense terminal connected to ground, there will be a residual collector current of approximately 300µA. If this is objectionable, insert a diode between current sense and ground.

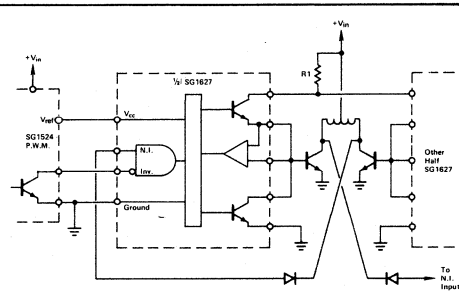


Figure 6. Simultaneous conduction of the output switching transistors can be positively prevented by using diodes to cross-couple a gating signal into the non-inverting inputs. For maximum power handling capability, the source transistor is driven into saturation with the current limiting provided by R1.

Data subject to change without notice.

HIGH-CURRENT FLOATING SWITCH DRIVER

SG1629/SG3629

DESCRIPTION

The SG1629 and SG3629 are monolithic integrated circuits designed to generate the positive and negative base drive currents (I_{b1} and I_{b2}) required for high-speed, high power switching transistors. These units are intended to interface between the secondary of a drive transformer and the base of an NPN switching device. Positive drive current can be made constant with an external programming resistor, or can be clamped with a diode to keep the switching device out of saturation. Negative turn-off current is derived from a negative voltage generated in an external capacitor. All operating power is supplied by the transformer secondary and these devices can be floated at high levels with respect to ground for off-line, bridge converters.

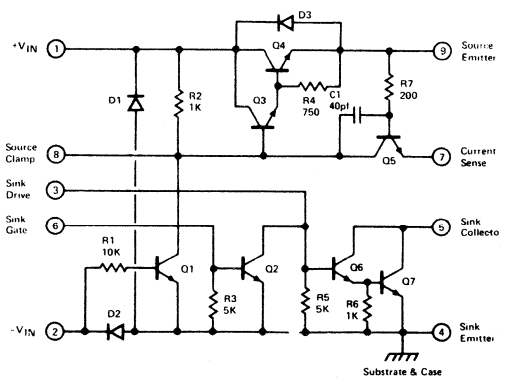
For medium power applications, these units are available in 10-pin, TO-100 package; while high power capability is offered in a 9-pin, TO-66 case. In either package , the SG1629 is specified for operation over an ambient temperature range of -55°C to +125°C while the SG3629 is intended for industrial applications of 0 to 70°C.

FEATURES

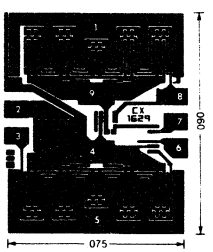
- **Self-generating positive and negative currents**
- **Constant source current (I_{b1}) to one amp**
- **Two amp peak sink current (I_{b2}) to negative voltage**
- **Floating operation**
- **Baker clamp input for non-saturated switching**
- **Provisions for source and sink gating**
- **100 nanosecond response**

3

SCHEMATIC



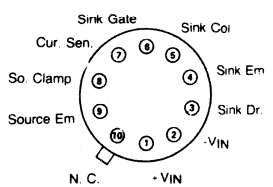
CHIP LAYOUT



CONNECTION DIAGRAMS

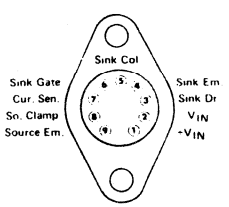
T-Package

TO-100



R-PACKAGE
TO-66

TOP VIEWS



Note: Case is internally connected to pin 4.

SEPTEMBER 1978

SG1629/SG3629

ABSOLUTE MAXIMUM RATINGS

Input Voltage + or - Inputs	20V
Collector to Emitter Voltage, Source or Sink	20V
Source Current	2.0 A
Sink Current	3.0 A
Sink Rectifier Current (peak)	2.0 A
Average Total Power Dissipation (Note 1)	
R-Package (TO-66)	3000 mW
Derate above 50°C	24 mW/°C
T-Package (TO-100)	680 mW
Derate above 50°C	5.4 mW/°C

Operating Junction Temperature Range	
SG1629	-55°C to +150°C
SG3629	0°C to +125°C
Storage Temperature Range	-65°C to +175°C

Note 1: Total power dissipation must include the power in both source and sink transistors times the duty cycle for each.

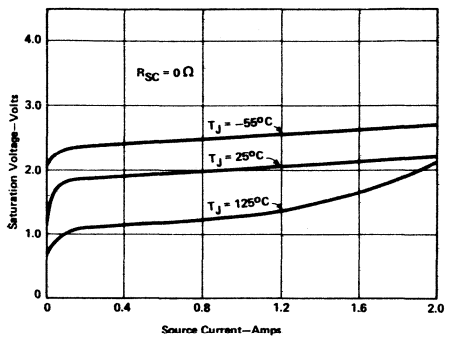
ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_J = −55°C to +150°C for the SG1629 and 0°C to 125°C for the SG3629.

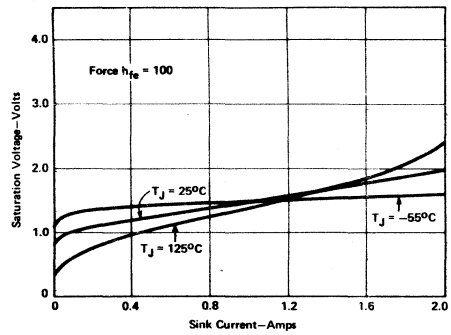
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Collector to Emitter Voltage Source or Sink	V_{BE} = 0		20	30	–	Volts
Collector to Emitter Leakage Source or Sink	V_{BE} = 0, V_{CE} = 15V		–	5	100	μA
Input Leakage V+ to V-	Input Voltage = +15V		–	1	100	μA
Input Leakage V- to V+	Input Voltage = -15V		–	2	4	mA
Standby Current from Sink Emitter Voltage	Sink Emitter = -5V 1kΩ from $-V_{IN}$ to Sink Drive Source Emitter Connected to Sink Collector $+V_{IN}$ = $-V_{IN}$ = 0V		–	5	10	mA
Clamp Current	$+V_{IN}$ = 15V V clamp = 0V		10	15	20	mA
Source Saturation Voltage	I source = 100 mA		–	1.7	–	Volts
	I source = 500 mA		–	1.8	–	Volts
	I source = 1A T_J = 25°C		–	2.0	3	Volts
Sink Saturation Voltage Force beta = 100	I sink = 100 mA		–	1.2	–	Volts
	I sink = 500 mA		–	1.3	–	Volts
	I sink = 1A T_J = 25°C		–	1.5	2	Volts
Sink Current Gain	I sink = 2A, V_{CE} = 3V		300	500	–	
Current Limit Sense Voltage	R_{SC} = 0.7Ω T_J = 25°C		0.55	0.65	0.80	Volts
Sink Rectifier Forward Voltage	I_F = 1A T_J = 25°C		–	1.0	2.0	Volts
Sink Gate Output Saturation	Sink Drive = 10 mA Sink Gate Input Current = 1 mA		–	0.2	0.4	Volts
Source Response	I source = 1A		–	100	–	nS
Sink Response	I sink = 1A		–	100	–	nS
Thermal Resistance	R-Package	θJA	–	40	–	°C/W
		θJC	–	5	–	°C/W
	T-Package	θJA	–	150	–	°C/W
		θJA	–	25	–	°C/W

SG1629/SG3629

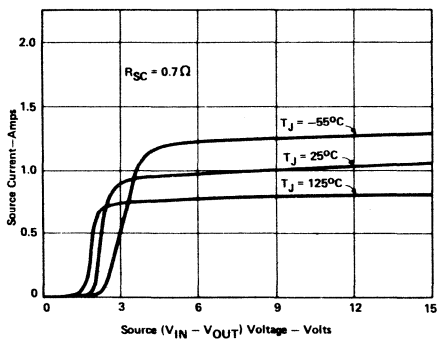
SOURCE SATURATION



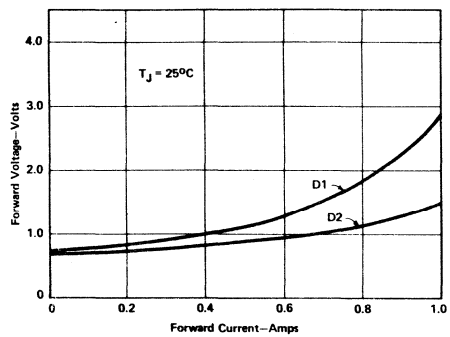
SINK SATURATION



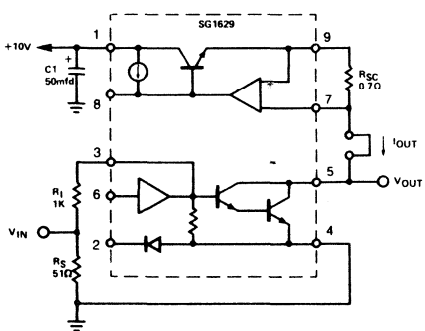
CONSTANT SOURCE CURRENT

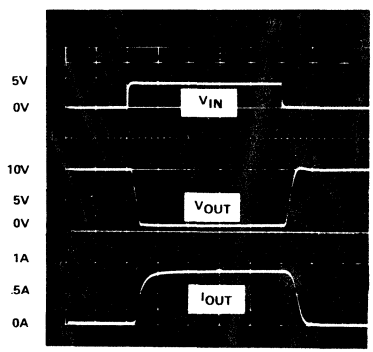


RECTIFIER FORWARD VOLTAGE



DYNAMIC RESPONSE





200 nS/Division

SG1629/SG3629

APPLICATIONS

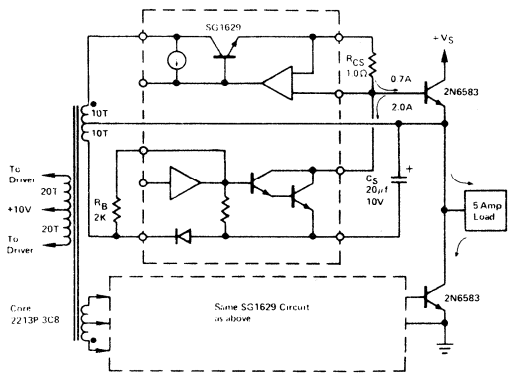


Figure 1. Two SG1629 devices can be combined to form the drive signals for the power transistors in a 5-amp, half-bridge switching supply.

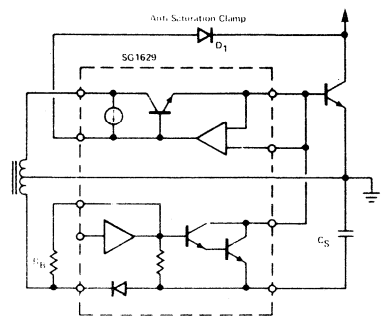


Figure 2. A load-dependent drive current may be provided by eliminating the current sensing resistor and adding the anti-saturation clamp diode D1.

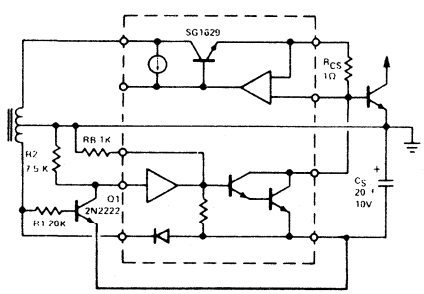


Figure 3. Where transformer inductance would normally degrade turn-on current rise time, the use of the sink gate with a relatively slow external transistor, Q1, will delay the sink turn-off until after source current has been established.

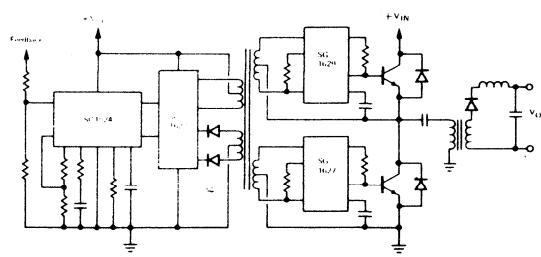


Figure 4. A simplified drive system for a half-bridge switched mode converter. A full bridge drive may be accommodated with four SG1629 drivers and additional current boosting for the SG1627.

SG7520/39 — High Speed Sense Amplifiers will detect bipolar differential signals from memory core arrays and provide logic-level outputs for interfacting with external logic. These devices are intended for systems requiring threshold voltage levels of ±15 mV to ±40 mV.

SG7520/21 — Two sense amplifiers are connected to a common output stage with capability of being flip-flop connected as part of the memory output register.

SG7522/23 — Two sense amplifiers are connected to a common output stage. Open collector output transistors may be used as wired-OR.

SG7524/25 — Two sense amplifiers with independent output stages.

SG7528/29 — Similar to SG7524/25 except analog test points are brought out.

SG7534/35 — Similar to the SG7524/25 except it has logically inverted outputs with open collectors for wired-OR.

SG7538/39 — Similar to the SG7528/29 except it has logically inverted outputs with open collectors for wired-OR.

SG55XX Series — Available for operation over full temperature range.

PARAMETERS[1]	CONDITIONS	SG7520, 21, 22, 23 24,25,28,29 34,35,38,39	UNITS
Operating Temperature Range	Free Air	0 to +70	°C
Package Types		J, N (16 pin)	°C
Differential Input Threshold Voltage (min/typ/max)[2]	V_{ref} = 15mV SG7520, 22, 24, 28, 34, 38	11/15/19	mV
	SG7521, 23, 25, 29, 35, 39	8/15/22	
	V_{ref} = 40mV SG7520, 22, 24, 28, 34, 38	36/40/44	
	SG7521, 23, 25, 29, 35, 39	33/40/47	
Common Mode Input Firing Voltage[3]	T_A = 25°C, Common Mode Input Pulse: $t_r = t_f \leq 15ns$, $t_{p(in)} = 50ns$	±2 (typ)	V
Differential Input Bias Current	$V^+ = 5.25V$, $V^- = -5.25V$, $V_{inD} = 0mV$	75	μA
Logical 1 Input Voltage (gate & strobe inputs)	$V^+ = 4.75V$, $V^- = -4.75V$, $V_{in(0)} = 0.8V$	2	V
Logical 0 Input Voltage (gate & strobe inputs)	$V^+ = 4.75V$, $V^- = -4.75V$, $V_{in(1)} = 2V$	0.8	V
Logical 0 Level Input Current (gate & strobe inputs)	$V^+ = 5.25V$, $V^- = -5.25V$, $V_{in(0)} = 0.4V$	−1.6	mA
Logical 1 Level Input Current (gate & strobe inputs)	$V^+ = 5.25V$, $V^- = -5.25V$, $V_{in(1)} = 2.4V$	40	μA
	(with $V_{in(1)} = V^+$)	1	mA
Logical 1 Output Voltage	$V+ = 4.75V$, $V- = -4.75V$, $I_{load} = -400\mu A$, $V_{in(1)} = 2V$, $V_{in(0)} = 0.8V$	2.4	V
Logical 0 Output Voltage	$V+ = 4.75V$, $V- = -4.75V$, $I_{sink} = 16mA$ $V_{in(0)} = 0.8V$	0.4	V
V+ Supply Current	T_A = 25°C	28 (typ)	mA
V− Supply Current	T_A = 25°C	−15 (typ)	mA
Output Short Circuit Current (except 7520/21Q)	$V+ = 5.25V$, $V- = -5.25V$	2.1/3.5	mA
Output Q Short Circuit Current 7520/21	$\lvert V^+ = 5.25V, V^- = 5.25V \rvert$	3.3/5.0	mA
Output Leakage Current (7522/23/34/35/38/39)	$V+ = 4.75V$, $V- = -4.75V$, $V_{out} = 5.25V$, $V_{in} = 2V$	250	μA
Differential Input Overload Recovery Time[4]	$V_{inD} = 2V$, $t_r = t_f = 20ns$ T_A = 25°C	20 (typ)	nS
Common Mode Input Overload Recovery Time[5]	$V_{inCM} = \pm 2V$, $t_r = t_f = 20ns$ T_A = 25°C	20 (typ)	nS
Minimum Cycle Time	T_A = 25°C	200 (typ)	nS

PROPAGATION DELAY TIMES (T_A = 25°C)	7520/21 (nS MAX) OUTPUT Q	OUTPUT $\bar{Q}$	7522/23	(nS MAX)	7524/25 7528/29	(nS MAX)	7534/35 7538/39	(nS MAX)
Input: $A_1 - A_2$ or $B_1 - B_2$	tpd(1)D (40)	tpd(0)D (55)	tpd(0)D	(45)	tpd(1)D	(40)	tpd(0)D	(40)
Input: Strobe A or B	tpd(1)S (30)	tpd(0)S (55)	tpd(0)S	(40)	tpd(1)S	(30)	tpd(0)S	(30)
Input: Gate Q	tpd(1)G_Q (20)	tpd(0)G_Q (30)	tpd(0)G	(25)				
Input: Gate $\bar{Q}$		tpd(1)$G_{\bar{Q}}$						

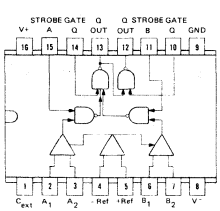
[1] Parameters are min./max. limits with V+ = 5V, V− = −5V, T_A = 0°C to +70°C unless otherwise specified.

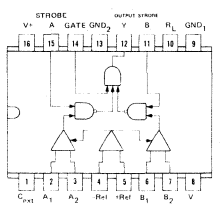
[2] V_T is defined as the d—c input voltage required to force the output of the sense amplifier to the logic gate threshold voltage level.

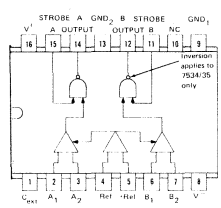
[3] V_{CMF} is the common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable signal present.

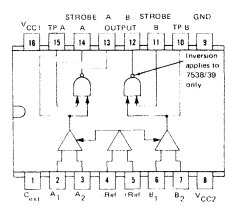
[4] Time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.

[5] Time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.









SG55138 / SG75138

Description:
The SG55138 and SG75138 Quad Bus Transceiver are designed for two way data communication over single ended transmission lines. Each of the four identical channels consists of a TTL input driver and a TTL output receiver. The driver output is of the open-collector type, and is designed to handle loads of up to 100 mA (50 ohms to 5V). The receiver input is internally connected to the driver output, and has a high impedance to minimize loading of the transmission line. Because of the high driver current, and the high receiver impedance, a very large number (typically hundreds) of transceivers may be connected to a single data bus. The receiver design also features a threshold of 2.3V (typical), providing a greater noise margin than would be possible with a TTL threshold receiver. This device also features a common driver strobe which turns off all drivers (high impedance), but does not affect receiver operation. This circuit is designed for operation from a single 5 volt supply, and it includes a provision to minimize loading of the data bus when the power supply voltage is zero. This circuit is available in the 16-pin ceramic (J) package. The SG75138 is characterized for industrial temperature range operation (0°C to 70°C), and the SG55138 is characterized for military temperature range operation (−50°C to 125°C).

Features:
- **Single 5V Supply**
- **High Threshold Receivers**
- **High Input Impedance Receivers**
- **Four Independent Channels**
- **Common Driver Strobe**
- **TTL/DTL Compatible Driver and Strobe Inputs With Clamp Diodes**
- **High Speed Operation**
- **100 mA Open-Collector Driver Outputs**
- **TTL Compatible Receiver Outputs**
- **Available in 16-Pin Ceramic (J) Packages**

Absolute Maximum Ratings

Supply voltage, Vcc	7.0V
Input voltage, V_{IN}	5.5V
Driver output sink current	150 mA
Storage temperature	−65°C to 150°C
Operating free air temperature,	
SG55138	−55°C to 125°C
SG75138	0°C to 70°C

3

Electrical Characteristics over recommended operating free-air temperature range.

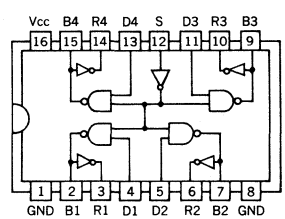
PARAMETER		TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	High Level Input Voltage, Driver or Strobe Inputs			2.0			V
$V_{IH(R)}$	High Level Input Voltage, Rec. Input	V_S = 2.0V, V_{OL} = 0.4V, I_{OL} = 16mA	SG55138	3.2			V
			SG75138	2.9			V
V_{IL}	Low Level Input Voltage, Driver or Strobe Inputs					0.8	V
$V_{IL(R)}$	Low Level Input Voltage, Rec. Input	V_S = 2.0V, V_{OH} = 2.4V, I_{OH} = 0.4mA	SG55138			1.5	V
			SG75138			1.8	V
V_{OH}	High Level Output Voltage, Rec. Output	Vcc = MIN., I_{OH} = −.4mA, $V_{IL(R)}$ = MAX, V_S = 2.0V		2.4	3.5		V
V_{OL}	Low Level Output Voltage, Rec. Output	Vcc = MIN., I_{OL} = 16mA, $V_{IH(R)}$ = MIN., V_S = 2.0V				400	mV
V_{OL}	Low Level Output Voltage, Driver Output	Vcc = MIN., I_{OL} = 100mA, V_S = 0.8V, V_D = 2.0V				450	mV
I_{IH}	High Level Input Current, Driver or Strobe Inputs	Vcc = MAX.	V_I = 2.4V			40	μA
			V_I = Vcc			1	mA
I_{IH}	High Level Input Current, Receiver Input	Vcc = 5.0V, V_I = 4.5V, V_S = 2.0V			25	300	μA
I_{IL}	Low Level Input Current Driver or Strobe Inputs	Vcc = MAX., V_I = 0.4V			−1	−1.6	mA
I_{IL}	Low Level Input Current, Receiver Input	Vcc = MAX., V_I = 0.45V, V_S = 2.0V				−50	μA
I_{OS}*	Short Circuit Output Current, Rec. Output	V_S = 0.8V, V_D = 2.0V, Vcc = MAX.		−18	−30	−55	mA
I_{CCL}	Supply Current, All Drivers On	Vcc = MAX., V_S = 0.8V, V_D = 2.0V			50	65	mA
I_{CCH}	Supply Current, All Drivers Off	Vcc = MAX., V_S = 2.0V, V_R = 3.5V			42	55	mA
R_{IN}	Input Current with Power Off, Receiver Input	Vcc = 0.0V, V_I = 4.5V			1.1	1.5	mA
V_{IC}	Input Clamp Voltage Strobe, Driver Inputs	Vcc = MIN., I_F = −12mA				−1.5	V

* Not more than one output at a time should be shorted.

Switching Characteristics, V_{CC} = 5.0V, T_A = 25°C

PARAMETER		TEST COND.	MIN.	NOM.	MAX.	UNITS
$t_{PLH(D-B)}$	Propagation delay, low to high level bus output from driver input.	V_S = 0.4V, C_L = 50pf, R_L = 50Ω, V_L = 5.0V		15	24	ns
$t_{PHL(D-B)}$	Propagation delay, high to low level bus output from driver input.			14	24	ns
$t_{PLH(S-B)}$	Propagation delay, low to high level bus output from strobe input.	V_D = 2.4V, C_L = 50pf, R_L = 50Ω, V_L = 5.0V		18	28	ns
$t_{PHL(S-B)}$	Propagation delay, high to low level bus output from strobe input.			22	32	ns
$t_{PLH(B-R)}$	Propagation delay, low to high level receiver output from bus input.	V_S = 2.4V, C_L = 15pf, R_L = 400Ω, V_L = 5.0V		7	15	ns
$t_{PHL(B-R)}$	Propagation delay, high to low level receiver output from bus input.			8	15	ns

LOGIC DIAGRAM

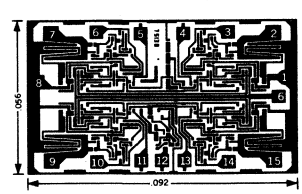


Positive logic: $B = \overline{D} + S$, $R = \overline{B}$

Recommended Operating Conditions

	MIN.	NOM.	MAX.	UNIT
Supply Voltage, Vcc, SG55138	4.5	5.0	5.5	V
Supply Voltage, Vcc, SG75138	4.75	5.0	5.25	V
Driver Output Low Current, $I_{OL(B)}$			100	mA
Receiver Output Low Current $I_{OL(R)}$			16	mA
Receiver Output High Current, $I_{OH(R)}$			−.4	mA
Operating Free-Air Temp., SG55138	−55		+125	°C
Operating Free-Air Temp., SG75138	0		+70	°C

CHIP LAYOUT



SG55154 / SG75154

Description

The SG55154 and SG75154 are monolithic Quadruple Line Receivers designed to meet the requirements of EIA Standard RS-232-C. These devices are intended to interface between data terminal equipment and communication equipment but they can also be used for many other types of relatively short, single-line, point-to-point data transmission systems. While these devices are normally operated from a single 5-volt supply, a built-in regulator allows operation to 12 volts without additional components.

Two forms of hysteresis are provided: For normal operation, the threshold-control terminals are connected to V_{CC1}, pin 15 and the circuit operates with a wide hysteresis loop which yields no change in the output should the inputs go to zero. In the fail-safe mode of operation, the threshold-control terminals are left open and the hysteresis loop is reduced such that the output will always go high if the input goes to zero.

These units are packaged in a 16-pin hermetic cerdip dual-in-line package. The SG55154 is rated for -55° to +125°C operation while the SG75154 is specified for operation over a 0° to +70°C range.

Features

- **Fail-safe capability with adjustable input threshold**
- **3 kΩ to 7 kΩ input resistance**
- **Outputs compatible with DTL or TTL**
- **Built-in hysteresis**
- **5V or 12V single supply operation**

Absolute Maximum Ratings

Normal Supply Voltage (pin 15)	7V
Alternate Supply Voltage (16 pin)	14V
Input Voltage to T_A = 70°C	±25V
to T_A = 125°C	± 10V
Operating Temperature Range	
SG55154	-55°C to 125°C
SG75154	0° to 70°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation	1000 mW
Derate above 25°C	8 mW/°C

3

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted) (See Note 1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX (SEE NOTE 2)	UNIT
V_{IH}	High-level input voltage			3			V
V_{IL}	Low-level input voltage					-3	V
V_{T+}	Positive-going threshold voltage	Normal operation		0.8	2.2	3	V
		Fail-safe operation		0.8	2.2	3	
V_{T-}	Negative-going threshold voltage	Normal operation		-3	-1.1	0	V
		Fail-safe operation		0.8	1.4	3	
$V_{T+}-V_{T-}$	Hysteresis	Normal operation		0.8	3.3	6	V
		Fail-safe operation		0	0.8	2.2	
V_{OH}	High-level output voltage		I_{OH} = -400 μA	2.4	3.5		V
V_{OL}	Low-level output voltage		I_{OL} = 16 mA		0.23	0.4	
r_I	Input resistance		ΔV_I = -25V to -10V*	3	5	7	kΩ
			ΔV_I = -10V to -3V	3	5	7	
			ΔV_I = -3V to 3V	3	6		
			ΔV_I = 3V to 10V	3	5	7	
			ΔV_I = 10V to 25V*	3	5	7	
$V_{I(open)}$	Open-circuit input voltage		I_I = 0	0	0.2	2	V
I_{OS}	Short-circuit output current**		V_{CC1} = 5.5V, V_I = -5V	-10	-20	-40	mA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 5.5V, T_A = 25°C		20	35	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC2} = 13.2V, T_A = 25°C		23	40	

*T_A = +70°C Maximum

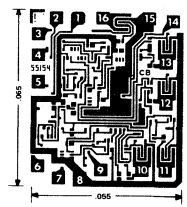
**Not more than one output should be shorted at a time.

NOTE 1: Above specifications guaranteed over -55°C < T_A < +125°C for SG55154 and 0° < T_A < 70°C for SG75154. All typical values are at V_{CC1} = 5V, T_A = 25°C.

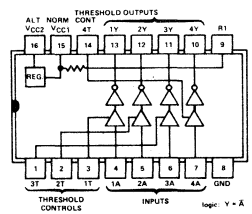
NOTE 2: The algebraic convention where the most-positive (least-negative) limit is designed as maximum is used in this data sheet for logic and threshold levels only, e.g., when -3V is the maximum, the minimum limit is a more-negative voltage.

Switching Characteristics, V_{CC1} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	C_L = 50 pF, R_L = 390 Ω		22		ns
t_{PHL}	Propagation delay time, high-to-low level output			20		ns
t_{TLH}	Transition time, low-to-high output			9		ns
t_{THL}	Transition time, high-to-low output			6		ns



CHIP LAYOUT



CONNECTION DIAGRAM

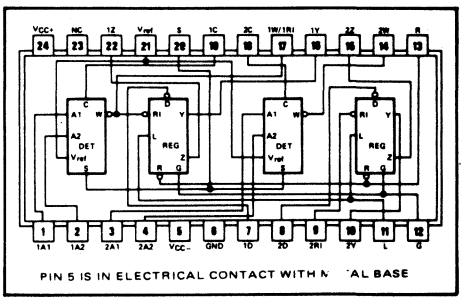
DUAL-IN-LINE PACKAGE (TOP VIEW)

SG55236
SG75236

ADVANCE DATA
Performance data described herein represent design goals.
Final device specifications are subject to change.

HIGH-SPEED SENSE AMPLIFIERS WITH BUILT-IN DATA REGISTER AND BUFFER FOR APPLICATION IN COINCIDENT-CURRENT CORE MEMORIES

- ± 2-mV Threshold Sensitivity with Threshold Voltage Independent of Temperature and Supply-Voltage Variations
- Adjustable Differential-Input Threshold Voltage
- Reference Amplifier Inherently Stable with No External Frequency Compensation Required
- Built-In Data Register with Provisions for External Data Inputs
- Built-In Data Buffer Drives 450-pF Load in 15 ns
- Low Power Consumption
- Internal Reference Voltage Attenuator Makes Reference Amplifier Less Sensitive to Noise
- Two Independent Channels with TTL Compatible Logic Inputs and Outputs



NC—No internal connection

3

FUNCTION TABLE

INPUTS								OUTPUTS	
A	C	S	W/RI†	L	D	R	G	Y	Z
H	H	H	L	X	X	X	H	H	L
H	H	H	L	X	X	X	L	H	H
↓	H	H	↑	L	X	H	H	H	L
↓	H	H	↑	L	X	H	L	H	H
H	↓	H	↑	L	X	H	H	H	L
H	↓	H	↑	L	X	H	L	H	H
H	H	↓	↑	L	X	H	H	H	L
H	H	↓	↑	L	X	H	L	H	H
L	X	X	H	H	H	X	X	L	H
L	X	X	H	H	L	X	H	H	L
L	X	X	H	H	L	X	L	H	H
L	X	X	H	L	X	L	X	L	H
L	X	X	H	L	X	↑	X	L	H
X	L	X	H	H	H	X	X	L	X
X	L	X	H	H	L	X	H	H	L
X	L	X	H	H	L	X	L	H	H
X	L	X	H	L	X	L	X	L	H
X	L	X	H	L	X	↑	X	L	H
X	X	L	H	H	H	X	X	L	X
X	X	L	H	H	L	X	H	H	L
X	X	L	H	H	L	X	L	H	H
X	X	L	H	L	X	L	X	L	H
X	X	L	H	L	X	↑	X	L	H

The normal sequence of operation is shown in the timing diagram.

FUNCTION TABLE FOR DUAL-CHANNEL DETECTOR OPERATION (2W connected to 1W/1R1)

INPUTS					OUTPUT
1A	1C	2A	2C	S	1W-2W
H	H	X	X	H	L
X	X	H	H	H	L
↓	H	L	X	H	↑
↓	H	X	L	H	↑
L	X	↓	H	H	↑
X	L	↓	H	H	↑
Any Other Combination					H

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high level to low level, ↑ = transition from low level to high level
†The W/RI column shows the output from the detector resulting from the inputs A, C, and S. In positive logic, W = $\overline{ACS}$. For dual operation with 2W connected to 2RI, this column represents an intermediate node and can be ignored.

For independent operation of register 2, this column is an input and the A, C, and S columns should be ignored.

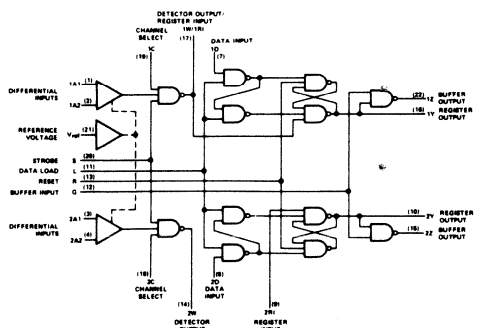
For dual-channel operation with 2W connected to 1W/1R1, this column is the result of W = $\overline{S(1A \cdot 1C + 2A \cdot 2C)}$ as shown in the table above.

definition of logic levels

INPUT	H	L
A‡	$V_{ID} > V_T$ max	$V_{ID} < V_T$ min
LOGIC	$V_I > V_{IH}$ min	$V_I < V_{IL}$ max

‡A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is consider positive regardless of which terminal is positive with respect to the other.

functional block diagram



SG55236
SG75236

ADVANCE DATA
Performance data described herein represent design goals. Final device specifications are subject to change.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		4.75	5	5.25	V
Supply voltage, V_{CC-}		−4.75	−5	−5.25	V
Reference voltage, V_{ref}		±1.5	±2.1	±4.5	V
High-level output voltage, V_{OH}	Detector and buffer			V_{CC}	V
High-level output current, I_{OH}	Register			−400	μA
Low-level output current, I_{OL}	Register			16	mA
	Buffer			25	
	Detector			3.2	
Width of reset pulse, $t_{w(R)}$		115			ns

Supply voltages (see Note 1)
- V_{CC+} . . . . . 7 V
- V_{CC-} . . . . . −7 V

Reference voltage, V_{ref} . . . . . ±5 V
Differential input voltage, V_{ID} . . . . . ±5 V
Voltage from any input to ground . . . . . 5.25 V
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 3) . . . . 450 mW
Operating free-air temperature range: SG 55236 . . . . . −55°C to 125°C
SG 75236 . . . . . 0°C to 70°C
Storage Temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds . . . . . 300°C

NOTE: 1. Voltage values, except differential input voltage, are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range, $V_{ref} = \pm 2.1$V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3)		V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C	SG55236	5	7	9	mV
				SG75236	4	7	10	
			V_{CC+} = 5 V ± 5%, V_{CC-} = −5 V ± 5%	SG55236	4.5	7	9.5	
			V_{CC+} = 5 V, V_{CC-} = −5 V	SG75236	4	7	10	
V_{ICF}	Common-mode input firing voltage		f = 0.1 MHz to 20 MHz			±1.5		V
I_{IB}	Differential-input bias current		V_{CC+} = 5 V, V_{CC-} = −5 V, V_{ID} = 0			20		μA
I_{IO}	Differential-input offset current		V_{CC+} = 5 V, V_{CC-} = −5 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe and logic inputs)				2			V
V_{IL}	Low-level input voltage (strobe and logic inputs)						0.8	V
V_{OH}	High-level output voltage	Register	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4			V
		Detector	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V					
I_{OH}	High-level output current	Buffer	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 4.75 V				250	μA
V_{OL}	Low-level output voltage	Register	V_{CC} = 4.75 V, V_{CC-} = −4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
		Buffer	V_{CC} = 4.75 V, V_{CC-} = −4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 25 mA				0.5	V
		Detector	V_{CC} = 4.75 V, V_{CC-} = −4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V				0.4	V
I_I	Input current at maximum input voltage (logic inputs)		V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IH}	High-level input current	Data in or channel select	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
		Register input 2RI					−750	
		Strobe, reset, or buffer input					80	
		Data load					160	
I_{IL}	Low-level input current	Strobe, reset, or buffer input	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V				−3.2	mA
		Register input 2RI					−3	
		Channel select					−1.6	
		Data load					−6.4	
		Data in					−2	
I_{OS}	Short-circuit output current‡	Register	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_O = 0		−20		−60	mA
I_{ref}	Reference-input current		V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ref} = −2.1 V, T_A = 25°C				0.5	mA
I_{CC+}	Supply current from V_{CC+}		V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C				55	mA
I_{CC-}	Supply current from V_{CC-}		V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C				18	mA

SG55325/SG75325

PERFORMANCE

- 600-mA Output Capability
- Fast Switching Times
- Output Short-Circuit Protection
- Dual Sink and Dual Source Outputs
- Minimum Time Skew between Address and Output Current Rise
- 24-Volt Output Capability

EASE OF DESIGN

- Source Base Drive Externally Adjustable
- TTL or DTL Compatibility
- Input Clamping Diodes
- Transformer Coupling Eliminated
- Reliability Increased
- Drive-Line Lengths Reduced
- Use of External Components Minimized

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SG55325	SG75325	UNIT
Supply voltage V_{CC1} (see Note 1)		7	7	V
Supply voltage V_{CC2} (see Note 1)		25	25	V
Input voltage (any address or strobe input)		5.5	5.5	V
Continuous total dissipation at (or below) 100°C case temperature		1	1	W
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTE: 1. Voltage values are with respect to network ground terminal.

electrical characteristics over rated operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SG55325 MIN	SG55325 TYP†	SG55325 MAX	SG75325 MIN	SG75325 TYP†	SG75325 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC1} = 4.5 V, I_I = −10 mA,	V_{CC2} = 24 V, T_A = 25°C		−1.3	−1.7		−1.3	−1.7	V
$I_{(off)}$	Source-collectors terminal off-state current		V_{CC1} = 4.5 V, V_{CC2} = 24 V	Full range			500			200	μA
				T_A = 25°C		3	150		3	200	
V_{OH}	High-level sink output voltage		V_{CC1} = 4.5 V, I_O = 0	V_{CC2} = 24 V,	19	23		19	23		V
$V_{(sat)}$	Saturation voltage	Source outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(source)}$ ≈ −600 mA,	Full range			0.9			0.9	V
				T_A = 25°C		0.43	0.7		0.43	0.75	
		Sink outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(sink)}$ ≈ 600 mA,	Full range			0.9			0.9	
				T_A = 25°C		0.43	0.7		0.43	0.75	
I_I	Input current at maximum input voltage	address inputs	V_{CC1} = 5.5 V, V_I = 5.5 V	V_{CC2} = 24 V,			1			1	mA
		strobe inputs					2			2	
I_{IH}	High-level input current	address inputs	V_{CC1} = 5.5 V, V_I = 2.4 V	V_{CC2} = 24 V,		3	40		3	40	μA
		strobe inputs				6	80		6	80	
I_{IL}	Low-level input current	address inputs	V_{CC1} = 5.5 V, V_I = 0.4 V	V_{CC2} = 24 V,		−1	−1.6		−1	−1.6	mA
		strobe inputs				−2	−3.2		−2	−3.2	
$I_{CC(off)}$	Supply current, all sources and sinks off	from V_{CC1}	V_{CC1} = 5.5 V, T_A = 25°C	V_{CC2} = 24 V,		14	22		14	22	mA
		from V_{CC2}				7.5	20		7.5	20	
I_{CC1}	Supply current from V_{CC1}, either sink on		V_{CC1} = 5.5 V, $I_{(sink)}$ = 50 mA,	V_{CC2} = 24 V, T_A = 25°C		55	70		55	70	mA
I_{CC2}	Supply current from V_{CC2}, either source on		V_{CC1} = 5.5 V, $I_{(source)}$ = −50 mA,	V_{CC2} = 24 V, T_A = 25°C,		32	50		32	50	mA

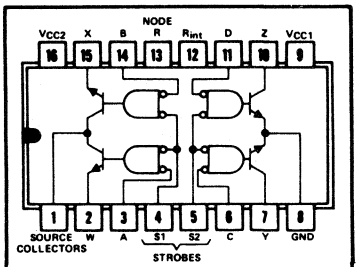
SG55325/SG75325

switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Source collectors	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		25	50	ns
t_{PHL}					25	50	
t_{TLH}	Source outputs	10	V_{CC2} = 20 V, R_L = 1 kΩ, C_L = 25 pF		55		ns
t_{THL}					7		
t_{PLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		20	45	ns
t_{PHL}					20	45	
t_{TLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		7	15	ns
t_{THL}					9	20	
t_s	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		15	30	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{TLH} = transition time, low-to-high-level output
t_{THL} = transition time, high-to-low-level output
t_s = storage time

J, OR N DUAL-IN-LINE
OR F FLAT PACKAGE (TOP VIEW)



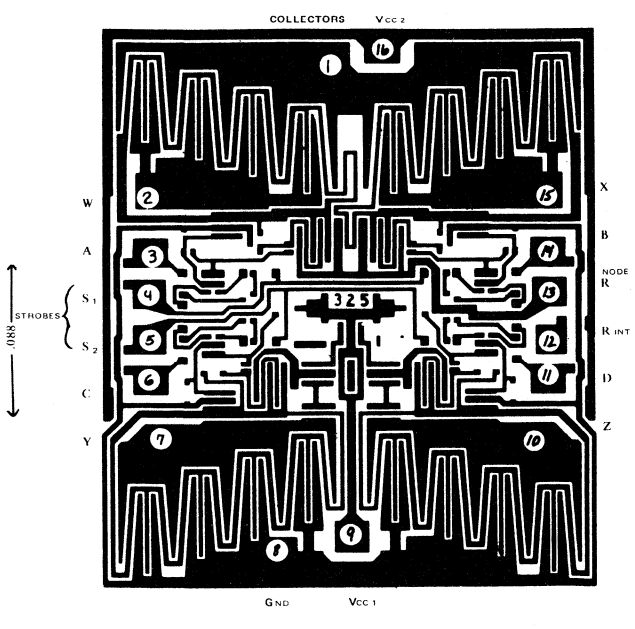
PIN 8 OF THE F FLAT PACKAGES IS IN ELECTRICAL CONTACT WITH THE METAL BASE

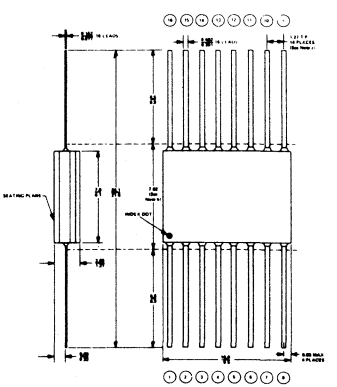
positive logic: See truth table

TRUTH TABLE

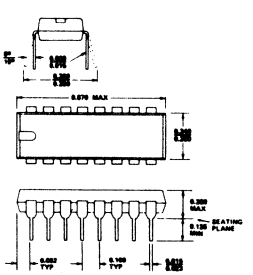
ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant
NOTE: Not more than one output is to be on at any one time.





F-FLAT PACKAGE
16 PIN CERAMIC



N-PACKAGE
16-PIN PLASTIC

3

SG55326/SG75326
SG55327/SG75327

FEATURES

- Quad Positive or Sink Memory Drivers
- 600 mA Output Current Sink Capability
- 24V Output Capability
- Clamp Voltage Variable to 24V
- SG55327, SG75327 PERFORMANCE
- Quad Memory Switches
- 600 mA Output Current Capability
- VCC2 Drive Voltage Variable to 24V
- Output Capable of Swinging Between VCC2 and Ground
- High-Repetition-Rate Driver Compatible with High-Speed Magnetic Memories
- Inputs Compatible with TTL Decoders
- Minimum Time Skew between Strobe and Output-Current Rise
- Pulse-Transformer Coupling Eliminated
- Drive-Line Lengths Reduced

ABSOLUTE MAXIMUM RATINGS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SG55326	SG75326	SG55327	SG75327	UNIT
Supply voltage, V_{CC} or V_{CC1} (see Note 1)	7	7	7	7	V
Supply voltage, V_{CC2}			25	25	V
Input voltage, any address or strobe	5.5	5.5	5.5	5.5	V
Output collector voltage	25	25	25	25	V
Output clamp voltage	25	25			V
Output collector current	750	750	750	750	mA
Continuous total dissipation at (or below) 100°C case temperature (see Note 2)	1	1	1	1	W
Operating free-air temperature range	−55 to 125	0 to 70	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds: J, Y or M package	300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260	260	260	260	°C

recommended operating conditions

	SG55326			SG75326			SG55327			SG75327			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} or V_{CC1}	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
Supply voltage, V_{CC2}							4.5		24	4.5		24	V
Output collector voltage			24			24			24			24	V
Output-clamp voltage, $V_{(clamp)}$	4.5		24	4.5		24							V
Output collector current			600			600			600			600	mA
Operating free-air temperature, T_A	−55		125	0		70	−55		125	0		70	°C

NOTE: 1. Voltage values are with respect to network ground terminal(s).

SG55326/SG75326 SG55327/SG75327

SG55326, SG75326 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SG55326			SG75326			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = 4.5 V, T_A = 25°C	I_I = −10 mA,		−1	−1.7		−1	−1.7	V
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_O = 0	19	23		19	23		V
$V_{(sat)}$	Saturation voltage		V_{CC} = 4.5 V, $I_{(sink)}$ = 600 mA§, See Note 3	Full range			0.9			0.9	V
				T_A = 25°C		0.43	0.7		0.43	0.75	
$V_{F(clamp)}$	Output-clamp-diode forward voltage		$V_{(clamp)}$ = 0, T_A = 25°C	$I_{(clamp)}$ = −10 mA,			1.5			1.5	V
$I_{(clamp)}$	Output-clamp current, one output on		$I_{(sink)}$ = 50 mA,	T_A = 25°C		5	7		5	7	mA
I_I	Input current at maximum input voltage	Address	V_I = 5.5 V				1			1	mA
		Strobe					4			4	
I_{IH}	High-level input current	Address	V_I = 2.4 V				40			40	μA
		Strobe					160			160	
I_{IL}	Low-level input current	Address	V_I = 0.4 V			−1	−1.6		−1	−1.6	mA
		Strobe				−4	−6.4		−4	−6.4	
$I_{CC(off)}$	Supply current, all outputs off		All inputs at 5 V,	T_A = 25°C		18	25		18	25	mA
$I_{CC(on)}$	Supply current, one output on		$I_{(sink)}$ = 50 mA,	T_A = 25°C		58	75		58	75	mA

SG55326, SG75326 switching characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
t_{PLH}	W, X, Y, or Z	V_S = $V_{(clamp)}$ = 15 V, R_L = 24 Ω, C_L = 25 pF, See Figure 5		30	50	ns
t_{PHL}				25	50	
t_{TLH}	W, X, Y, or Z			7	15	ns
t_{THL}				10	20	
t_s	W, X, Y, or Z			24	35	ns
V_{OH}	W, X, Y, or Z	V_S = $V_{(clamp)}$ = 24 V, R_L = 47 Ω, C_L = 25 pF, $I_{(sink)}$ ≈ 500 mA, See Figure 5	V_S−25			mV

SG55327, SG75327 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SG55327			SG75327			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = 4.5 V, T_A = 25°C	I_I = −10 mA		−1	−1.7		−1	−1.7	V
$I_{(off)}$	Collectors terminal off-state current		V_{CC1} = 4.5 V, $V_{(col)}$ = 24 V	Full range			500			200	μA
				T_A = 25°C			150			200	
$V_{(sat)}$	Saturation voltage		V_{CC1} = 4.5 V, V_O = 0, $I_{(source)}$ = −600 mA§, See Notes 3 and 4	Full range			0.9			0.9	V
				T_A = 25°C		0.43	0.7		0.43	0.75	
I_I	Input current at maximum input voltage	Address	V_I = 5.5 V				1			1	mA
		Strobe					4			4	
I_{IH}	High-level input current	Address	V_I = 2.4 V				40			40	μA
		Strobe					160			160	
I_{IL}	Low-level input current	Address	V_I = 0.4 V			−1	−1.6		−1	−1.6	mA
		Strobe				−4	−6.4		−4	−6.4	
$I_{CC(off)}$	Supply current, all outputs off	From V_{CC1}	All inputs at 5 V,	T_A = 25°C		7	10		7	10	mA
		From V_{CC2}				13	20		13	20	
$I_{CC(on)}$	Supply current, one output on	From V_{CC1}	$V_{(col)}$ = 6 V,	$I_{(source)}$ = −50 mA,		8	12		8	12	mA
		From V_{CC2}	T_A = 25°C,	See Note 3		36	55		36	55	

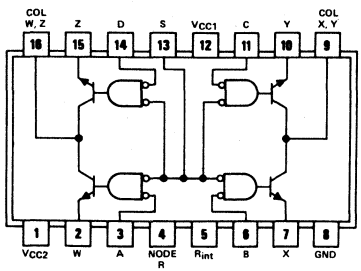
SG55327, SG75327 switching characteristics, V_{CC1} = 5V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
t_{PLH}	Collectors	V_S = V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF, See Figure 5 and Note 4		35	55	ns
t_{PHL}	W, Z or X, Y			30	55	
t_{TLH}	W, X, Y, or Z	$V_{(col)}$ = V_{CC2} = 20 V, R_L = 100 Ω, C_L = 25 pF, See Figure 6 and Note 4		30		ns
t_{THL}				10		
V_{OH}	Collectors W, Z or X, Y	V_S = V_{CC2} = 24 V, R_L = 47 Ω, C_L = 25 pF, $I_{(sink)}$ ≈ 500 mA, See Figure 5 and Note 4	V_S−25			mV

SG55326/SG75326
SG55327/SG75327

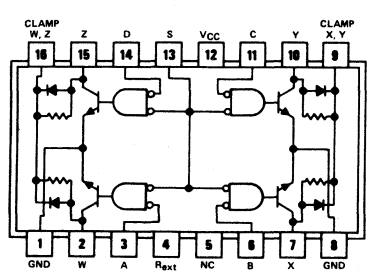
CONNECTION DIAGRAMS

SG55327, SG75327
J OR N DUAL-IN-LINE OR
SB FLAT PACKAGE (TOP VIEW)



PIN 8 OF Y AND M PACKAGES IS IN ELECTRICAL CONTACT WITH THE METAL BASE

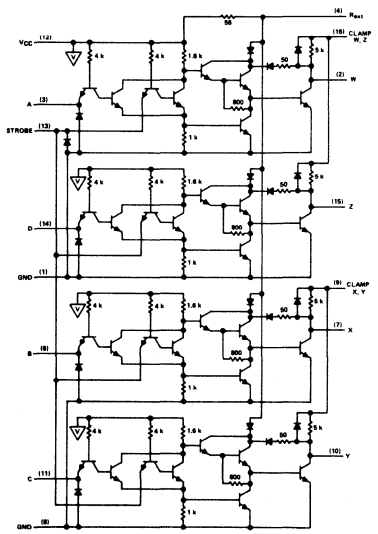
SG55326, SG75326
J OR N DUAL-IN-LINE OR
F FLAT PACKAGE (TOP VIEW)



PINS 1 AND 8 OF Y AND M PACKAGES ARE IN ELECTRICAL CONTACT WITH THE METAL BASE

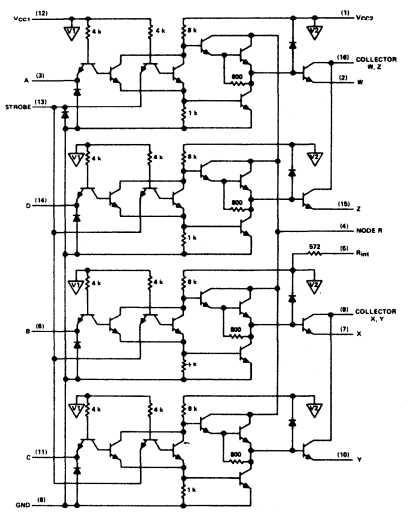
SCHEMATICS

SG55326, SG75326



▽ ▽ ▽ . . . V_{CC}, V_{CC1}, or V_{CC2} bus, respectively.

SG55327, SG75327

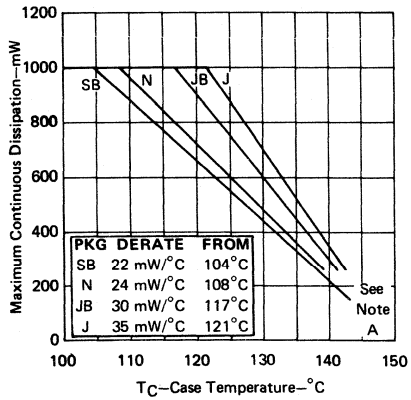


Resistor values shown are nominal and in ohms.

SG55326/SG75326
SG55327/SG75327

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE



NOTE A: Rated operating free-air temperature ranges must be observed regardless of heat-sinking.

FIGURE 1

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

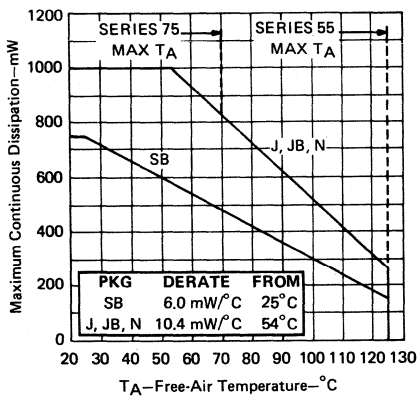
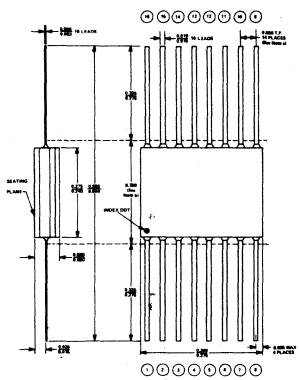
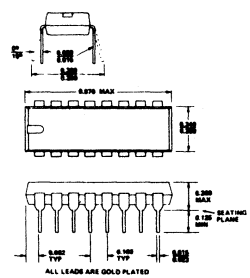


FIGURE 2

PACKAGES



F-FLAT PACKAGE
16-PIN CERAMIC



N-PACKAGE
16-PIN PLASTIC

J-PACKAGE
16-PIN CERDIP

SG55450B/75450B SG55460/75460

The SG55450B and SG55460 Series are general purpose dual peripheral drivers whose output stage includes a completely uncommitted, high-voltage, high current NPN transistor. Inputs to the standard TTL gates are diode clamped and fully DTL/TTL compatible. The output transistors of the SG55450B and SG75450B are capable of sinking 300 mA and will withstand 30 volts when off. The SG55460 and SG75460 devices have the same current rating but with higher voltage capability of 40 volts and only slight reduction in switching speeds.

The SG55450B and SG55460 are characterized for operation over the full military temperature range of -55°C to +125°C while the SG75450B and SG75460 are designed for 0°C to +70°C operation.

- **Current capacity of 300 mA per driver**
- **High output voltage capability**
- **High-speed switching characteristics**
- **Both military and commercial temperature ranges**

ABSOLUTE MAXIMUM RATINGS (Note 1)	SG55450B SG75450B	SG55460 SG75460
Supply Voltage, V_{CC}	7V	7V
Input Voltage	5.5V	5.5V
V_{CC} to Substrate Voltage	35V	40V
Collector to Substrate Voltage	35V	40V
Collector to Base Voltage	35V	40V
Collector to Emitter Voltage (Note 2)	30V	40V
Emitter to Base Voltage	5V	5V
Collector Current (Note 3)	300mA	300mA
Power Dissipation		
N Package (plastic)	600mW	600mW
Derate above 25°C	6.0mW/°C	6.0mW/°C
J Package (cerdip)	1000mW	1000mW
Derate above 25°C	6.7mW/°C	6.7mW/°C
Operating, Free Air Temperature Range		
SG55450B, SG55460	−55°C to +125°C	
SG75450B, SG75460	0°C to +70°C	
Storage Temperature Range	−65°C to +150°C	

NOTES:
1. Voltage values shown are with respect to ground terminal unless otherwise specified.
2. With base-to-emitter resistance less than 500Ω.
3. Both sides of circuit may conduct rated current simultaneously provided power dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

(over operating temperature range and with V_{CC} = 5V ± 5%, unless otherwise specified)

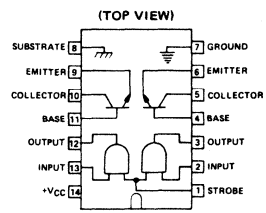
3

TTL GATES

Parameter	Test Conditions	Min.	Typ.	Max.	Units
High-level input voltage, V_{IH}	V_{OL} < 0.4V, I_{OL} = 16mA	2	—	—	V
Low-level input voltage, V_{IL}	V_{OH} > 2.4V, I_{OH} = −.4mA	—	—	0.8	V
High-level output voltage, V_{OH}	V_{IL} = 0.8V, I_{OH} = −.4mA	2.4	3.3	—	V
Low-level output voltage, V_{OL}	V_{IH} = 2.0V, I_{OL} = 16 mA	—	.25	0.4	V
Input clamp voltage, V_I	I_I = −12mA	—	−1.2	−1.5	V
High-level input current, I_{IH}	V_I = 2.4V	—	—	40	μA
High-level strobe current, I_{SH}	V_I = 2.4V	—	—	80	μA
Low-level input current, I_{IL}	V_I = 0.4V	—	—	−1.6	mA
Low-level strobe current, I_{SL}	V_I = 0.4V	—	—	−3.2	mA
Input current at max. V, I_I	V_I = 5.5V	—	—	1.0	mA
Strobe current at max. V, I_S	V_S = 5.5V	—	—	2.0	mA
Output short circuit current, I_{OS}		−18	−35	−55	mA
Supply current, high out, I_{CCH}	V_I = 0	—	2	4	mA
Supply current, low out, I_{CCL}	V_I = 5V	—	6	11	mA

OUTPUT TRANSISTORS (High current measurements made with pulse techniques)

Parameter	Test Conditions	55450B	75450B	55460	75460	Units
Collector-base breakdown BV_{CBO}	I_C = 100μA, I_E = 0	35	35	40	40	V min.
Collector-emitter breakdown BV_{CER}	I_C = 100μA, R_{BE} = 500Ω	30	30	40	40	V min.
Emitter-base breakdown BV_{EBO}	I_E = 100μA, I_C = 0	5	5	5	5	V min.
Base-emitter voltage V_{BE}	I_B = 10mA, I_C = 100 mA	1.2	1.0	1.2	1.0	V max.
	I_B = 30mA, I_C = 300 mA	1.4	1.2	1.4	1.2	V max.
Collector-emitter saturation $V_{CE\ (SAT)}$	I_B = 10mA, I_C = 100mA	.5	.4	.5	.4	V max.
	I_B = 30mA, I_C = 300mA	.8	.7	.8	.7	V max.
Current transfer ratio h_{FE}	V_{CE} = 3V, I_C = 100mA, T_A = 25°C	25	25	25	25	min.
	V_{CE} = 3V, I_C = 300mA, T_A = 25°C	30	30	30	30	min.
	V_{CE} = 3V, I_C = 100mA, T_A = min.	10	20	10	20	min.
	V_{CE} = 3V, I_C = 300 mA, T_A = min.	15	25	15	25	min.

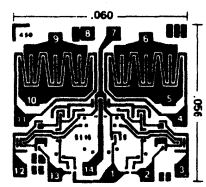


CONNECTION DIAGRAM

Note: The substrate (pin 8) must always be at the most negative voltage for proper device operation.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

Parameter	Test Conditions	55450B, 75450B Typ.	55450B, 75450B Max.	55460, 75460 Typ.	55460, 75460 Max.	Units
TTL GATES						
Propagation delay time Low-to-high-level output, t_{PLH}	C_L = 15 pF	12	22	22	—	nS
Propagation delay time High-to-low-level output, t_{PHL}	R_1 = 400Ω	8	15	8	—	nS
OUTPUT TRANSISTORS						
Delay time, t_d	I_C = 200mA	8	15	10	—	nS
Rise time, t_r	$I_{b(1)}$ = 20mA $I_{b(2)}$ = −40mA	12	20	16	—	nS
Storage time, t_s	$V_{BE(OH)}$ = −1V	7	15	23	—	nS
Fall time, t_f	C_L = 15 pF, R_L = 50Ω	6	15	14	—	nS
GATES & TRANSISTORS COMBINED						
Propagation delay time Low-to-high-level out, t_{PLH}	I_C = 200mA	20	30	45	65	nS
High-to-low-level out, t_{PHL}	C_L = 15 pF	20	30	35	50	nS
Transition time Low-to-high-level out, t_{TLH}	R_L = 50Ω	7	12	10	20	nS
High-to-low-level out, t_{THL}		9	15	10	20	nS



CHIP BONDING DIAGRAM

TRANSISTOR ARRAYS

SG2001 / SG2002 / SG2003

Description

These high voltage, medium current driver arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 600mA are allowable, making them ideal for driving tungsten filament lamps also.

Three different input configurations provide optimized designs for interfacing with TTL, DTL, PMOS, or CMOS drive signals.

In all cases, the individual Darlington pair collector current rating is 500mA. However, outputs may be paralleled for higher load current capability. All devices are supplied in a 16-pin dual in-line ceramic package.

Absolute Maximum Ratings (at 25°C free-air temperature for any one Darlington unless otherwise noted).

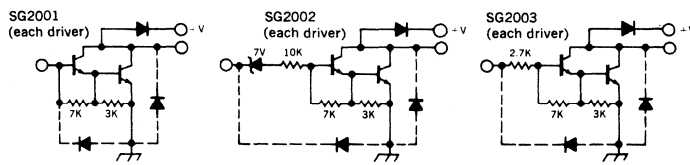
Output Voltage, V_{CE}	50V
Input Voltage, V_{in}	20V
Peak Collector Current, IC	600mA
Continuous Collector Current, IC	500mA
Continuous Base Current, IB	25mA
Power Dissipation, PD (per device)	1.0W
Total Package* Limitation	2.0W
Derating Factor above 25°C	13mW/°C
Ambient Temperature Range (Operating) TA	−55°C to +125°C
Storage Temperature Range, TS	−65°C to +175°C

*Under normal operating conditions, these units will sustain 350mA per output with VCC = 1.6V at 70°C with a pulse width of 20ms and a duty cycle of 30%.

Features

- **Collector currents to 600mA**
- **Low saturation voltage**
- **High speed switching**
- **Closely matched parameters**

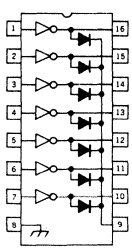
PARTIAL SCHEMATICS



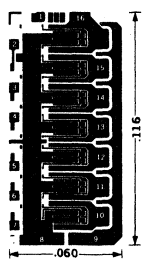
Electrical Characteristics at 25°C (unless otherwise noted)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50V; T_A = 70°C		100	μA
Collector-Emitter Saturation Voltage	V_{CE} (Sat)	I_C = 350mA; I_B = 500μA I_C = 100mA; I_B = 250μA		1.6 1.1	V V
Input Current Type SG-2002 Type SG-2003	I_{in} on	 V_{in} = 17V V_{in} = 3.85V		 1.3 1.35	 mA mA
Input Current SG-2002	I_{in} off	V_{in} = 6V, T_A = 70°C		50	μA
Input Voltage Type SG-2002 Type SG-2003	V_{in} on	 V_{CE} = 2V; I_C = 350mA V_{CE} = 2V; I_C = 350mA		 13 3.5	 V V
DC Forward Current Transfer Ratio Type SG-2001	h_{FE}	 V_{CE} = 2V; IC = 350mA	 1000		
Input Capacitance	C_{in}			30	pf
Turn-On Delay	t_{PLM}	0.5E_{in} to 0.5E_{out}		5	μS
Turn-Off Delay	t_{PHL}	0.5E_{in} to 0.5E_{out}		5	μS
Clamp Diode Leakage Current	I_R	V_R = 50V		50	μA
Clamp Diode Forward Voltage	V_F	I_F = 350mA		2.0	V

CONNECTION DIAGRAM

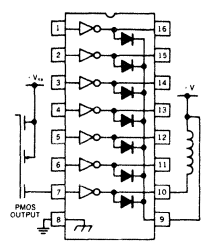


CHIP LAYOUT

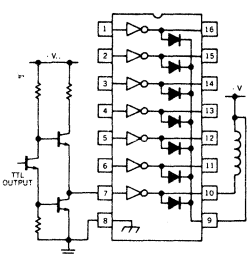


TYPICAL APPLICATIONS

PMOS TO LOAD



TTL TO LOAD



SG3018/3018A/3821/3822/3823/3086

(CA3018/3018A) (CA3045, 3046) (CA3026/3054) (CA3086)

These transistor arrays offer V_{BE} typically matched to ±0.5 mV, less than 10% variation in hfe, operation from dc to 300 MHz, high current gain from 10 μA to 10 mA and high voltage capability.

SG3018/SG3018A (CA3018, 3018A) Darlington Transistor Pairs – consists of four monolithic transistors. Two of the four are internally connected into a Darlington configuration with a typical current gain of 4000. The other two transistors are separate conventional types.

SG3821 (CA3046, 3045) Matched Transistor Array – five general purpose monolithic NPN transistors internally connected to form two independent differential amplifiers, each with its associated current source transistor.

SG3822 (CA3026, 3054) Dual Differential Transistors – six monolithic NPN transistors internally connected to form two independent differential amplifiers, each with its associated current source transistor.

SG3823 Dual Darlington Transistor Array – six monolithic transistors. Four are internally connected as two independent Darlington Amplifiers with a typical gain of 4000. The other two transistors are separate conventional types.

ABSOLUTE MAXIMUM RATINGS

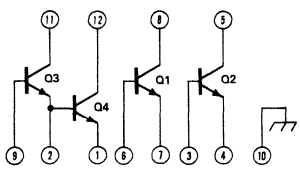
Collector-substrate Voltage 40V (CA Series 20V)
Collector-base Voltage 40V (CA Series 20V)
Collector-emitter Voltage 25V (CA Series 15V)
Emitter-base Voltage 5V
Collector-Current 50mA
Operating Temperature Range 0–125°C (CA Series 0 - 70°C)

PARAMETERS*	CONDITIONS	3018, 3018A, 3821, 3822, 3823,	CA3018/3026/3054 3045/3046/3086	UNITS
Collector-Substrate Breakdown	I_C = 10μA, I_B = 0	40	20	V
Collector-Base Breakdown	I_C = 10μA, I_E = 0	40	20	V
Collector-Emitter Breakdown	I_C = 100μA, I_B = 0	25	15	V
Emitter-Base Breakdown	I_E = 10μA, I_C = 0	5	5	V
Collector-Substrate Leakage	V_{CS} = 20V, I_B = 0	80	80	nA
Collector-Base Leakage	V_{CB} = 20V, I_E = 0	40	40	nA
Collector-Emitter Leakage	V_{CE} = 20V, I_B = 0	500	500	nA
Forward Current-Transfer Ratio	V_{CE} = 5V, I_C = 10μA	80 (typ)	80 (typ)	–
Forward Current-Transfer Ratio	V_{CE} = 5V, I_C = 1mA	50/400	50/400	–
Forward Current-Transfer Ratio	V_{CE} = 5V, I_C = 10mA	80 (typ)	80 (typ)	–
Collector-Emitter Saturation	I_C = 10mA, I_B = 1mA	0.5 (typ)	0.5 (typ)	V
Gain-Bandwidth Product	V_{CE} = 5V, I_C = 3mA	500 (typ)	500 (typ)	MHz
Collector-Substrate Capacitance	V_{CS} = 5V, I_C = 0	2.0 (typ)	2.0 (typ)	pF
Collector-Base Capacitance	V_{CB} = 5V, I_C = 0	0.4 (typ)	0.4 (typ)	pF
Noise Figure	f = 1kc, V_{CE} = 5V, I_C = 100μA, R_S = 1kΩ	4 (typ)	4 (typ)	dB
Input Offset Voltage for any two transistors	V_{CE} = 5V, I_C = 1mA	5	5	mV
Input Offset Current for any two transistors	V_{CE} = 5V, I_C = 1mA	4	2	μA
Forward Current Transfer Ratio (Darlington Pair), SG3018/3018A/3823	V_{CE} = 5V, I_C = 1mA	1500	1500	–

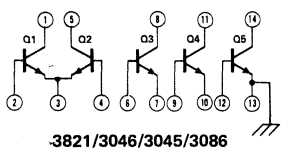
*Parameters apply for T_A = 25°C and are min/max limits unless otherwise specified.

Note: Substrate pin (⫽) must be connected to the most negative DC potential -- which should also be a good AC ground -- for proper isolation between transistors.

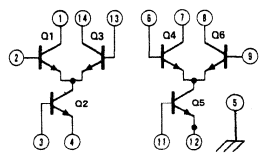
SG3018/3018A is offered in 12-pin metal can. All other 3800 Series arrays are offered in N and J 14-pin dual-in-line packages.



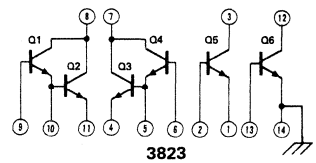
3018/3018A



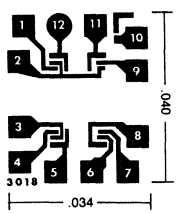
3821/3046/3045/3086

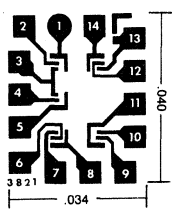


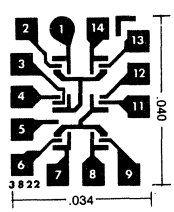
3822/3026/3054

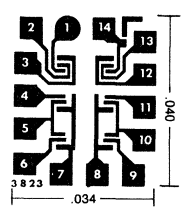


3823









SG3081/3082

The SG3081 and SG3082 each have seven high-current silicon NPN transistors integrated into a single monolithic chip. The SG3081 has all seven emitters common while the SG3082 is connected in a common collector configuration. Both devices have a separate substrate pin for more versatile applications. With current capability to 100 mA per transistor, these arrays are ideally suited for driving all types of seven-segment displays as well as other general purpose driver applications.

- **Collector current to 100mA**
- **Low saturation voltage**
- **Closely matched parameters**

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:			
Any one transistor		**500**	**mW**
Total package**		**750**	**mW**
Above 25°C	**Derate linearly**	**6.67**	**mW/°C**
Ambient Temperature Range:			
Operating		**–40 to +85**	**°C**
Storage		**–55 to +150**	**°C**

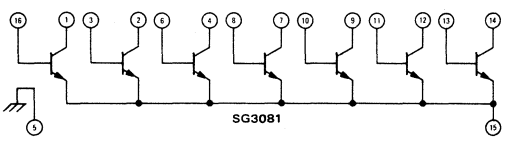
The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage (V_{CEO})	**16**	**V**
Collector-to-Base Voltage (V_{CBO})	**20**	**V**
Collector-to-Substrate Voltage (V_{CSO})	**20**	**V**
Emitter-to-Base Voltage (V_{EBO})	**5**	**V**
Collector Current (I_C)	**100**	**mA**
Base Current (I_B)	**20**	**mA**

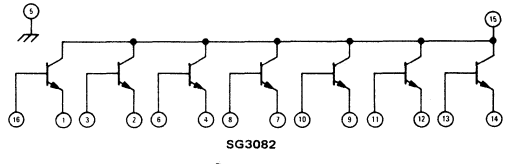
**SG3081 and SG3082 are available in N and J 16-Pin dual-in-line packages

PARAMETERS*	SYMBOL	CONDITIONS	SG3081/SG3082	UNITS
Collector-Base Breakdown Voltage	BV_{CBO}	I_C = 500μA, I_E = 0	20	V
Collector-Substrate Breakdown Voltage	BV_{CSO}	I_{CI} = 500μA, I_E = 0, I_B = 0	20	V
Collector-Emitter Breakdown Voltage	BV_{CEO}	I_C = 1mA, I_B = 0	16	V
Emitter-Base Breakdown Voltage	BV_{EBO}	I_C = 500μA	5	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 5.0 V, I_C = 30mA V_{CE} = 5.0 V, I_C = 50mA	50 40	
Base-Emitter Saturation Voltage	V_{BEsat}	I_C = 30mA, I_B = 1mA	1.0	V
Collector-Emitter Saturation Voltage:				
SG3081, SG3082		I_C = 30mA, I_B = 1mA	0.5	
SG3081	V_{CEsat}	I_C = 50mA, I_B = 5mA	0.7	V
SG3082		I_C = 50mA, I_B = 5mA	0.8	
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	1	μA

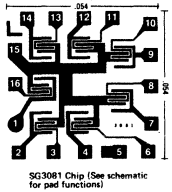
*Parameters are for T_A = 25°C and are min/max limits.



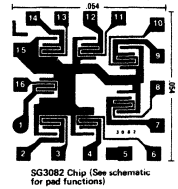
SG3081



SG3082



SG3081 Chip (See schematic for pad functions)



SG3082 Chip (See schematic for pad functions)

NOTE: Substrate pin (▨) must be connected to the most negative DC potential — which should also be a good AC ground — for proper isolation between transistors.

SG3083 SG3183/3183A

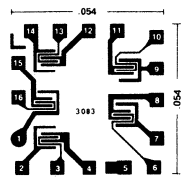
This series of arrays consists of five closely-matched, high current NPN transistors. Although sharing a common monolithic substrate, the transistors are connected such that all terminals are independent, including the substrate bias connector. With current capability to 100 mA per transistor, these arrays are ideally suited for all types of driving applications including relays, lamps, and thyristors. The SG3183 and SG3183A are higher voltage versions of the SG3083.

FEATURES

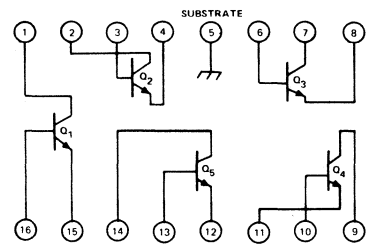
- **High voltage capability**
- **Collector current to 100 mA**
- **Low saturation voltage**
- **Closely matched parameters**

ABSOLUTE MAXIMUM RATINGS

Power Dissipations:	
Any one transistor	500 mW
Total package	750 mW
Above 25°C derate linearly	6.67 mW/°C
Ambient Temperature Range:	
Operating (N-Package)	−40 to +85°C
Operating (J-Package)	−55 to +125°C
Storage (both packages)	−65 to +150°C
Maximum Collector Current	100 mA
Maximum Base Current	20 mA



SG3083 Chip (See schematic for pad functions)



NOTE: The collector of each transistor is isolated from the substrate by an integral diode which must be reverse biased by connecting the substrate to a voltage more negative than any collector. To prevent undesired coupling between transistors, the substrate connection should be connected to an AC or DC ground.

4

ELECTRICAL CHARACTERISTICS AT TA = 25°C

PARAMETER SYMBOL CONDITIONS	MIN.	TYP.	MAX.	UNITS
Collector-Substrate Breakdown Voltage, BV_{CSO}, I_C = 100 μA				
SG3083	20	60	–	V
SG3183	40	70	–	V
SG3183A	50	70	–	V
Collector-Base Breakdown Voltage, BV_{CBO}, I_C = 100 μA				
SG3083	20	60	–	V
SG3183	40	70	–	V
SG3183A	50	70	–	V
Collector-Emitter Breakdown Voltage, BV_{CEO}, I_C = 1 mA				
SG3083	15	24	–	V
SG3183	30	40	–	V
SG3183A	40	50	–	V
Emitter-Base Breakdown Voltage, BV_{EBO}, I_E = 100 μA				
All types	5	6.9	–	V
Collector Cutoff Current, I_{CEO}, V_{CE} = 10V	–	–	10	μA
Collector Cutoff Current, I_{CBO}, V_{CR} = 10V	–	–	1	μA
DC Forward Current Transfer Ratio, h_{FE}				
All types V_{CE} = 3V, I_C = 10 mA	50	100	–	
V_{CE} = 5V, I_C = 50 mA	40	75	–	
Collector-Emitter Saturation Voltage, V_{CE} (SAT)				
SG3083 I_C = 50 mA, I_B = 5 mA	–	0.40	0.70	V
SG3183 /SG3183A I_C = 50 mA, I_B = 5 mA	–	1.7	3.0	V
Base to Emitter Voltage, V_{BE}, V_{CE} = 3V, I_C = 10 mA	0.65	0.75	0.85	V
For Q_1 and Q_2 Matched Pair				
Input Offset Voltage $\lvert V_{IO}\rvert$ V_{CE} = 3V, I_C = 1 mA	–	1.2	5	mV
Input Offset Current $\lvert I_{IO}\rvert$ V_{CE} = 3V, I_C = 1 mA	–	0.7	2.5	μA

SG3851 / SG3852 / SG3853

Description

These high voltage, high current Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 750mA are allowable, making them ideal for driving tungsten filament lamps also.

Three different input configurations provide optimized designs for interfacing with TTL, DTL, PMOS, or CMOS drive signals.

In all cases, the individual Darlington pair collector current rating is 600mA. However, outputs may be paralleled for higher load current capability. All devices are supplied in a 16-pin dual in-line ceramic package.

Absolute Maximum Ratings (at 25°C free-air temperature for any one Darlington unless otherwise noted).

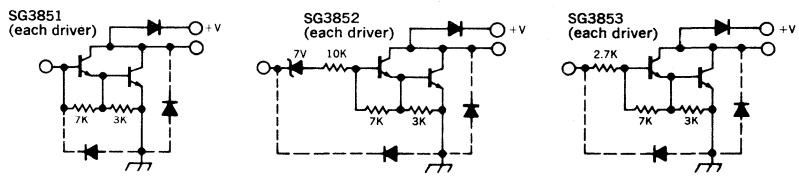
Output Voltage, V_{CE}	50V
Input Voltage, V_{in}	25V
Peak Collector Current, IC	750mA
Continuous Collector Current, IC	600mA
Continuous Base Current, IB	25mA
Power Dissipation, PD (per device)	1.0W
Total Package* Limitation	2.0W
Derating Factor above 25°C	13mW/°C
Ambient Temperature Range (Operating) TA	−55°C to +125°C
Storage Temperature Range, TS	−65°C to +175°C

*Under normal operating conditions, these units will sustain 350mA per output with VCC = 1.6V at 70°C with a pulse width of 20ms and a duty cycle of 30%.

Features

- **Collector currents to 750mA**
- **Low saturation voltage**
- **High speed switching**
- **Closely matched parameters**

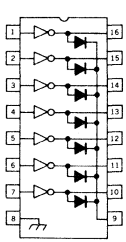
PARTIAL SCHEMATICS



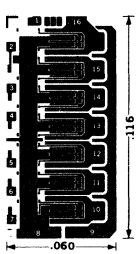
Electrical Characteristics at 25°C (unless otherwise noted)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50V; T_A = 70°C		100	μA
Collector-Emitter Saturation Voltage	V_{CE} (Sat)	I_C = 500mA; I_B = 800μA I_C = 100mA; I_B = 250μA		2.0 1.1	V V
Input Current Type SG-3852 Type SG-3853	I_{in} on	 V_{in} = 24V V_{in} = 5.0V		 3.0 3.0	 mA mA
Input Current SG-3852	I_{in} off	V_{in} = 6V, T_A = 70°C		50	μA
Input Voltage Type SG-3852 Type SG-3853	V_{in} on	 V_{CE} = 2V; I_C = 500mA V_{CE} = 2V; I_C = 350mA		 17 3.5	 V V
DC Forward Current Transfer Ratio Type SG-3851	h_{FE}	 V_{CE} = 2V; IC = 350mA	 1000		
Input Capacitance	C_{in}			30	pf
Turn-On Delay	t_{PLM}	0.5E_{in} to 0.5E_{out}		0.5	μS
Turn-Off Delay	t_{PHL}	0.5E_{in} to 0.5E_{out}		0.5	μS
Clamp Diode Leakage Current	I_R	V_R = 50V		50	μA
Clamp Diode Forward Voltage	V_F	I_F = 500mA		3.0	V

CONNECTION DIAGRAM

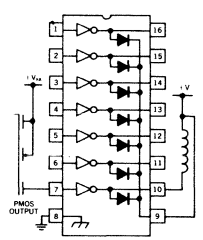


CHIP LAYOUT

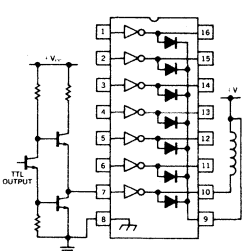


TYPICAL APPLICATIONS

PMOS TO LOAD



TTL TO LOAD



OTHER CIRCUITS

Video Amplifiers

Wideband Amplifiers/Multipliers

Wideband Video Amplifiers

Multipliers

Modulators

Zero Voltage Switches

Timers

Dual Timers

High-Voltage Fluorescent Display Driver

SG555/SG555C

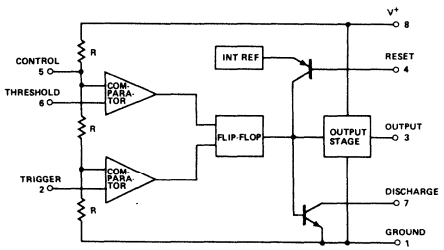
The SG555 integrated circuit has been designed to generate accurate time delays with provisions for remote triggering or resetting. An external resistor and capacitor will provide precise control of time delays from microseconds to hours. This circuit can also be used as a stable oscillator with accurate control of both frequency and duty cycle through the use of two external resistors and a single capacitor. The output circuit is designed for use with load currents to 200 mA and is fully compatible with TTL circuitry.

- **Direct replacement for SE555/NE555**
- **Both astable and monostable mode of operation**
- **Timing range from microseconds through hours**
- **200 mA output capability (source or sink)**
- **.005%/°C temperature stability**
- **TTL compatible**

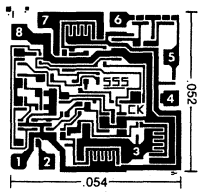
ABSOLUTE MAXIMUM RATINGS:

Supply Voltage	+18V
Power Dissipation	
T–Package (TO–99)	680mW
Derate above 25°C	5.4mW/°C
M–Package (Minidip)	400mW
Derate above 25°C	4.0mW/°C
Operating Temperature Range	
SG555	–55°C to +125°C
SG555C	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

FUNCTIONAL DIAGRAM



CHIP BONDING DIAGRAM

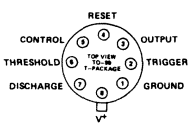


ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = +5V to +15V unless otherwise specified)

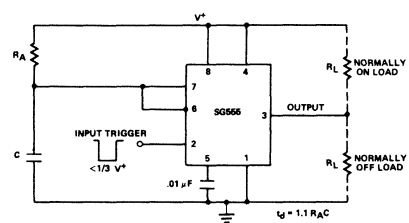
Parameter	Conditions	SG555 Min.	SG555 Typ.	SG555 Max.	SG555C Min.	SG555C Typ.	SG555C Max.	Units
Supply Voltage		4.5	—	18	4.5	—	16	V
Supply Current	V^+ = 5V, R_L = ∞	—	3	5	—	3	6	mA
	V^+ = 15V, R_L = ∞	—	10	12	—	10	15	mA
	Low State (Note 1)							
Timing Error	R_A, R_B = 1KΩ to 100KΩ							
Initial Accuracy	C = 0.1μF (Note 2)	—	0.5	2	—	1	—	%
Drift with Temperature		—	30	100	—	50	—	ppm/°C
Drift with Supply Voltage		—	0.005	0.2	—	0.01	—	%/Volt
Threshold Voltage		—	2/3	—	—	2/3	—	X V^+
Trigger Voltage	V^+ = 15V	4.8	5	5.2	—	5	—	V
	V^+ = 5V	1.45	1.67	1.9	—	1.67	—	V
Trigger Current		—	0.5	—	—	0.5	—	μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current		—	0.1	—	—	0.1	—	mA
Threshold Current	(Note 3)	—	0.1	.25	—	0.1	.25	μA
Control Voltage Level	V^+ = 15V	9.6	10	10.4	9.0	10	11	V
	V^+ = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drop (low)	V^+ = 15V							
	I_{SINK} = 10mA	—	0.1	0.15	—	0.1	.25	V
	I_{SINK} = 50mA	—	0.4	0.5	—	0.4	.75	V
	I_{SINK} = 100 mA	—	2.0	2.2	—	2.0	2.5	V
	I_{SINK} = 200mA	—	2.5	—	—	2.5	—	V
	V^+ = 5V							
	I_{SINK} = 8mA	—	0.1	0.25	—	—	—	V
	I_{SINK} = 5mA	—	—	—	—	.25	.35	V
Output Voltage Drop (high)								
	I_{SOURCE} = 200mA V^+ = 15V	—	12.5	—	—	12.5	—	V
	I_{SOURCE} = 100mA							
	V^+ = 15V	13.0	13.3	—	12.75	13.3	—	V
	V^+ = 5V	3.0	3.3	—	2.75	3.3	—	V
Rise Time of Output		—	100	—	—	100	—	nsec
Fall Time of Output		—	100	—	—	100	—	nsec

Note 1: Supply Current when output high typically 1mA less.
Note 2: Tested at V^+ = 5V and V^+ = 15V.
Note 3: This will determine the maximum value of R_A + R_B. For 15V operation, the max total R = 20 megohm.

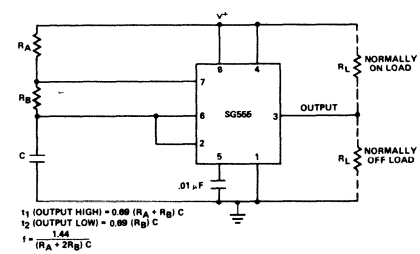
CONNECTION DIAGRAMS



APPLICATIONS



MONOSTABLE OPERATION



ASTABLE OPERATION

SG556/SG556C

The SG556/SG556C IC timing circuit is the equivalent of two 555-type timers in one 14-pin dual-in-line package. Each section of the device is capable of producing accurate time delays or oscillations. A resistor and a capacitor are the only external parts needed to control time delays from microseconds through hours. For use as an oscillator, two external resistors and a capacitor provide control of the free running frequency and duty cycle. Triggering and resetting terminals are provided and the circuit will trigger and reset on falling waveforms.

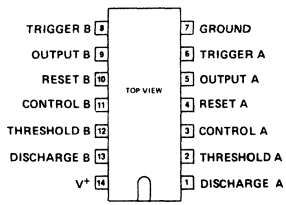
The SG556/SG556C Dual Timer lowers over-all system cost, reduces board space and assembly time required and provides matching and tracking characteristics which are superior to two separate timers.

- **Direct replacement for SE556/NE556**
- **Both astable and monostable mode of operation**
- **Timing range from microseconds through hours**
- **200 mA output capability (source or sink)**
- **.005%/°C temperature stability**
- **TTL compatible**

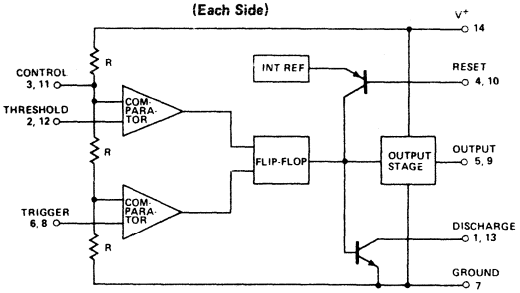
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
Power Dissipation	
N—Package (plastic)	600 mW
Derate above 25°C	6.0 mW/°C
J—Package (cerdip)	1000 mW
Derate above 25°C	6.7 mW/°C
Operating Temperature Range	
SG556	-55°C to +125°C
SG556C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM
(Each Side)

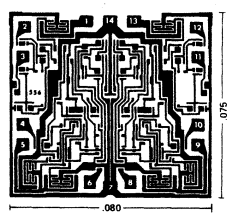


ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = +5 to +15 V unless otherwise specified)

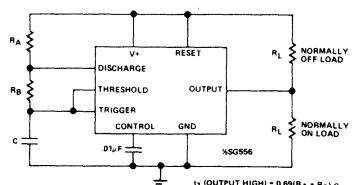
Parameter	Conditions	SG556 Min.	SG556 Typ.	SG556 Max.	SG556C Min.	SG556C Typ.	SG556C Max.	Units
Supply Voltage		4.5	—	18	4.5	—	16	V
Supply Current (each side)	V^+ = 5 V, R_L = ∞	—	3	5	—	3	6	mA
	V^+ = 15 V, R_L = ∞ Low State (Note 1)	—	10	11	—	10	14	mA
Timing Error (Monostable)	R_A, R_B = 2 kΩ to 100 kΩ C = 0.1 μF (Note 2)							
Initial Accuracy		—	0.5	1.5	—	0.75	—	%
Drift with Temperature		—	30	100	—	50	—	ppm/°C
Drift with Supply Voltage			0.05	0.2	—	0.1	—	%/Volt
Timing Error (Free Running)	R_A, R_B = 2 kΩ to 100 kΩ C = 0.1 μF (Note 2)							
Initial Accuracy		—	1.5	—	—	2.25	—	%
Drift with Temperature		—	90	—	—	150	—	ppm/°C
Drift with Supply Voltage		—	0.15	—	—	0.3	—	%/Volt
Threshold Voltage		—	2/3	—	—	2/3	—	X V^+
Trigger Voltage	V^+ = 15 V	4.8	5	5.2	4.5	5	5.6	V
	V^+ = 5 V	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger Current		—	0.5	—	—	0.5	—	μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current		—	0.1	—	—	0.1	—	mA
Threshold Current	(Note 3)	—	0.03	0.1	—	0.03	0.1	μA
Control Voltage Level	V^+ = 15 V	9.6	10	10.4	9.0	10	11	V
	V^+ = 5 V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drop (low)	V^+ = 15 V							
	I_{SINK} = 10 mA	—	0.1	0.15	—	0.1	0.25	V
	I_{SINK} = 50 mA	—	0.4	0.5	—	0.4	0.75	V
	I_{SINK} = 100 mA	—	2	2.25	—	2	2.75	V
	I_{SINK} = 200 mA	—	2.5	—	—	2.5	—	V
	V^+ = 5 V							
	I_{SINK} = 8 mA	—	0.1	0.25	—	—	—	V
	I_{SINK} = 5 mA	—	—	—	—	0.25	0.35	V
Output Voltage (high)	I_{SOURCE} = 200 mA V^+ = 15 V	—	12.5	—	—	12.5	—	V
	I_{SOURCE} = 100 mA V^+ = 15 V	13	13.3	—	12.75	13.3	—	V
	V^+ = 5 V	3	3.3	—	2.75	3.3	—	V
Rise Time of Output		—	100	—	—	100	—	ns
Fall Time of Output		—	100	—	—	100	—	ns
Discharge Leakage Current		—	20	100	—	20	100	nA
Matching Characteristics Between Each Section								
Initial Timing Accuracy		—	0.05	0.1	—	0.1	0.2	%
Timing Drift with Temperature		—	±10	—	—	±10	—	ppm/°C
Drift with Supply Voltage		—	0.1	0.2	—	0.2	0.5	%/Volt

NOTES: (1) Supply current when output is high is typically 1.0 mA less. (2) Tested at V^+ = 5 V and V^+ = 15 V.
(3) This will determine the maximum value of R_A + R_B. For 15 V operation, the maximum total R = 20 meg-ohms.

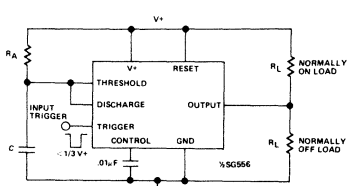
CHIP BONDING DIAGRAM



APPLICATIONS



ASTABLE OPERATION



MONOSTABLE OPERATION

SG733/733C

The SG733/733C are monolithic two-stage wideband amplifiers. These devices offer excellent gain stability at any gain setting and provide fixed gain options of 10, 100 and 400 without external components. All stages are current source biased to obtain high common mode and power supply rejection and emitter followers are used at the output to minimize the effects of capacitive loading. The devices are particularly well suited for applications requiring a fast linear function such as video and pulse amplifiers.

- **120MHz bandwidth**
- **Gain options of 10, 100, 400 without external components**
- **250kΩ input resistance**
- **No external frequency compensation necessary**

PARAMETERS*	733	733C	UNITS
Supply Voltage	±6V	±6V	V
Operating Temperature Range	−55 to +125	0 to +70	°C
Package Types	T, J	T, J, N	—
Differential Voltage Gain			
Gain 1[1]	300/500	250/600	V/V
Gain 2[2]	90/110	80/120	
Gain 3[3]	9/11	8/12	
Bandwidth			
Gain 1	40 (typ)	40 (typ)	MHz
Gain 2 (R_s = 50Ω)	90 (typ)	90 (typ)	
Gain 3	120 (typ)	120 (typ)	
Risetime			
Gain 2, R_s = 50Ω, V_{out} = $1V_{p-p}$	10	12	nS
Propagation Delay			
Gain 2, R_s = 50Ω, V_{out} = $1V_{p-p}$	10	10	nS
Input Resistance			
Gain 2	20	10	kΩ
Input Capacitance			
Gain 2	2 (typ)	2 (typ)	pF
Input Offset Current	3	5	μA
Input Bias Current	20	30	μA
Input Voltage Range	±1	±1	V
Common Mode Rejection Ratio			
Gain 2 V_{cm} ± 1V, f ≤ 100kHz	60	60	dB
V_{cm} ± 1V, f = 5MHz	60 (typ)	60 (typ)	
Supply Rejection Ratio			
Gain 2 ΔV_s = ±0.5V	50	50	dB
Output Offset Voltage			
Gain 1	1.5	1.5	V
Gain 2, Gain 3	1.0	1.5	
Output Common Mode Voltage	2.4/3.4	2.4/3.4	V
Output Voltage Swing	3	3	V_{p-p}
Output Sink Current	2.5	2.5	mA
Output Resistance	20 (typ)	20 (typ)	Ω
Power Supply Current	24	24	mA

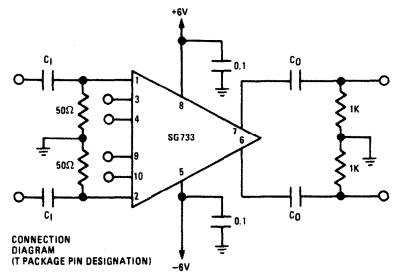
*Parameters apply for V_s = ±6V, at 25°C only and are min/max limits unless otherwise specified.

[1] Gain Select pins G_{1A} and G_{1B} connected together.

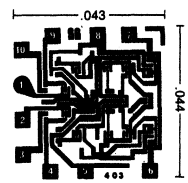
[2] Gain Select pins G_{2A} and G_{2B} connected together.

[3] All Gain Select pins open.

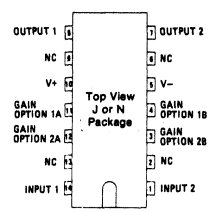
CONNECTION DIAGRAMS

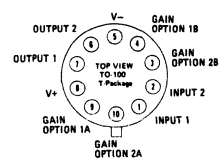


CONNECTION DIAGRAM (T PACKAGE PIN DESIGNATION)



SG733/733C Chip (See T-package diagram for pad functions)





SG1401/2401/3401

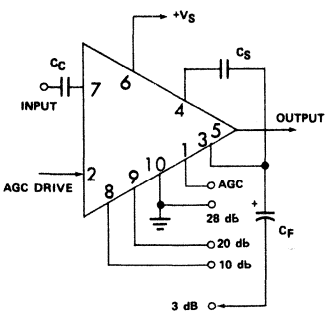
The SG1401/2401/3401 video amplifiers are useful over a frequency range from DC to 200MHz. Internal emitter followers are used to achieve high input and low output impedances, allowing simple capacitor coupling. Biasing and gain-setting resistors are internally diffused, eliminating external resistor networks. The gain may be externally varied through the use of AGC diodes which are included in the circuit.

- **20dB voltage gain at 100MHz**
- **5nsec rise and fall times**
- **Fixed or variable gain**
- **Single power supply voltage**
- **Minimum external components**
- **Symmetrical limiting**

PARAMETERS/CONDITIONS*	1401	2401	3401	UNITS
Operating Temperature Range	−55 to +125	0 to +70	0 to +70	°C
Package Types	T, J	T, J, N		–
Supply Voltage	6/20		6/20	V
Power Consumption, no AGC voltage	110		120	mW
DC Output Voltage	8.7 (typ)		8.7 (typ)	V
Peak-to-Peak Output, Pin 3 (4) to AC gnd	4 (typ)		3 (typ)	V
Voltage Gain, Pin 3 (4)[2] open	2.2/3.2		2.2/3.2	dB
Voltage Gain, Pin 3 (4)[2] coupled to Pin 8 (11)[2]	9/11		9/11	dB
Voltage Gain, Pin 3 (4)[2] coupled to Pin 9 (12)[2]	18/21		18/21	dB
Voltage Gain, Pin 3 (4)[2] to AC gnd	26/31		24/31	dB
Unity Gain Frequency, Pin 3 (4)[2] to AC gnd	200 (typ)		200 (typ)	MHz
Input Resistance, 20 dB gain	2.5 (typ)		2.5 (typ)	kΩ
Output Resistance, 20 dB gain	25 (typ)		50 (typ)	Ω
Input Capacitance, 20 dB gain	5 (typ)		5 (typ)	pF
Maximum Power Gain, 20 dB gain, R_L = 50Ω	30 (typ)		30 (typ)	dB
Temperature Stability, 20 dB gain	±1[1]		±2[1]	dB
AGC Range	20 (min)		22 (typ)	dB
Noise Figure, 20 dB gain, R_S = 1k	8 (min)		6 (typ)	dB

*Parameters apply only for T_A = 25°C, V_S = +12V, and f = 1 MHz, and are min/max limits unless otherwise specified.

[1]Over operating temperature range. [2]Numbers in parentheses refer to dual-in-line package.

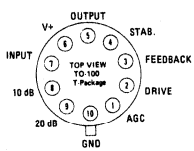


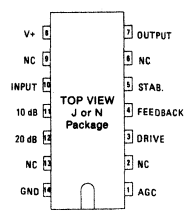
$$C_F = \frac{1}{2\pi f_c R}$$

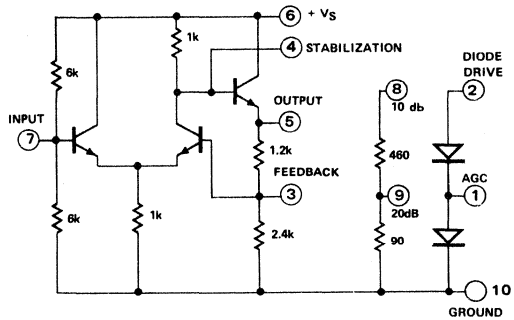
where f_c is low frequency corner and R is the gain setting resistance.

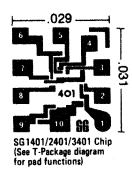
C_S = 0 to 10 pF to minimize high frequency peaking.

CONNECTION DIAGRAMS









See Applications Notes for additional information.

SG1402/2402/3402

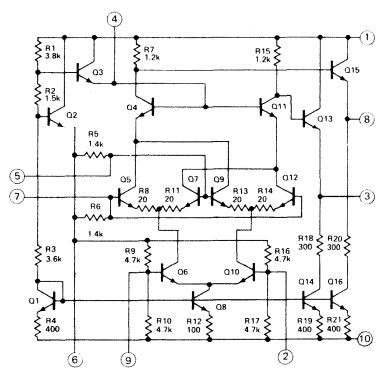
SG1402/2402/3402 are monolithic four quadrant multipliers offering excellent frequency response and provision for use as a variable gain amplifier with both non-inverting and inverting outputs available. In addition to linear amplification, the device is also ideal for balanced modulation, pulse or gated amplification, and coincidence detection.

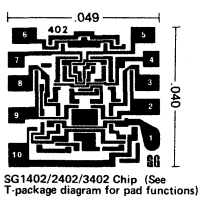
- **Single power supply voltage**
- **Self-contained biasing**
- **25dB voltage gain**
- **Differential or single ended inputs and outputs**
- **Large bandwidth**
- **Low power dissipation**

PARAMETERS, CONDITIONS*	1402	2402	3402	UNITS
Supply Voltage	+18		+18	V
Load Current	15		15	mA
Operating Temperature Range	−55 to +125	0 to +70	0 to +70	°C
Package Types	J, T	J, T, N		–
Maximum Voltage Gain, single ended	23		20	dB
Variable Gain Range, with ext. balance	55		40	dB
Frequency Response, f − 3 dB	40 (min)		50 (typ)	MHz
Input Impedance, Pin 5 or 7 (7 or 10)[1]	1.2 (typ)		1.2 (typ)	KΩ
Input Impedance, Pin 2 or 9 (3 or 12)[1]	1.8 (typ)		1.8	KΩ
Output Impedance, Pin 3 or 8 (4 or 11)[1]	100 (typ)		100 (typ)	Ω
Output Voltage Swing R_L = 100K R_L = 1K	 3 1.3		 3 1.3	Vpp
Quiescent DC Levels Pins 5, 6 and 7 (7, 8 & 10)[1]	3.6 (typ)		3.6 (typ)	V
Pins 2 and 9 (3 & 12)[1]	1.8 (typ)		1.8 (typ)	V
Pins 3 and 8 (4 & 11)[1]	6.5/7.5		7.0 (typ)	V
Output Offset Voltage Minimum Gain Maximum Gain	 100 200		 300 500	mV
DC Output Shift, with max gain change	100		200	mV
Differential Control Voltage, for max gain change	200 (typ)		200 (typ)	mV
Maximum Gain Variation, over temperature	2		3	dB
Equivalent Input Noise (BW = 10MHz, R_S = 50Ω)	25 (typ)		25	μVrms
Power Consumption	85		85	mW

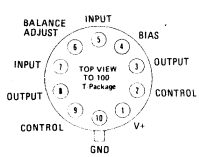
*Parameters are for T_A = 25°C, V^+ = 10V, f = 100KHz and are min./max. limits unless otherwise specified.

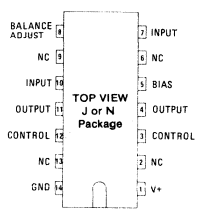
[1]Numbers in parentheses refer to dual-in-line package.





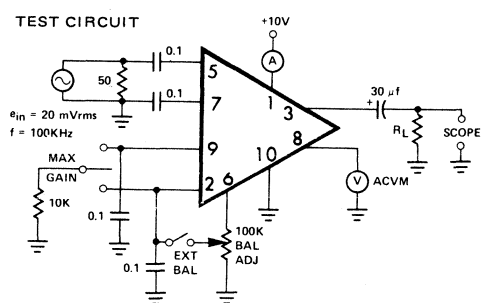
SG1402/2402/3402 Chip (See T-package diagram for pad functions)





CONNECTION DIAGRAMS

TEST CIRCUIT



See Applications Notes for additional information.

SG1595/1495

The SG1595/1495 four quadrant analog multipliers are designed for applications where the output voltage required is a linear product of two input voltages. Both types provide excellent linearity and operation over a wide supply range and input voltage range. Applications include use as multipliers, dividers, squarers, phase detectors, frequency doublers and as balanced modulators.

- **Excellent linearity**
- **Adjustable scale factor**
- **Excellent temperature stability**
- **Wide bandwidth**
- **High input voltage range**
- **Wide supply voltage operation**

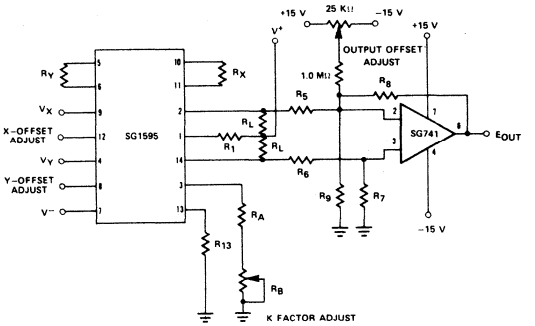
PARAMETERS/CONDITIONS*	1595	1495	UNITS
Operating Temperature Range	−55 to +125	0 to +70	°C
Package Types	J	J, N	—
Applied Voltage[2]	30	30	V
Differential Input Signal	$V_9 - V_{12} = \pm(6 + I_{13}R_X)$ $V_4 - V_8 = \pm(6 + I_3 R_Y)$		—
Maximum Factor Adjust Current	10	10	mA
Linearity Error in Percent of Full Scale (T_A = 25°C) $-10 < V_x < +10$ ($V_y = \pm 10V$) $-10 < V_y < +10$ ($V_x = \pm 10V$)	 1.0 2.0	 2.0 4.0	 (% max)
Squaring Mode Error T_A = 25°C T_A = 0°C to +70°C T_A = −55°C to +125°C	 0.5 — 0.75	 0.75 1.0 —	 (% typ)
Scale Factor (adjustable) $K = \frac{2R_L}{I_3 R_X R_Y}$	0.1 (typ)	0.1 (typ)	—
Input Resistance[1]	35 (typ)	20 (typ)	MΩ
Differential Output Resistance[1]	300 (typ)	300 (typ)	KΩ
Input Bias Current	8.0	12	μA
Input Offset Current	1.0	2.0	μA
Common Mode Gain	−50	−40	dB
Output Common Mode Voltage	21 (typ)	21 (typ)	V
Differential Output Voltage Swing	±14 (typ)	±14 (typ)	V
Pos Supply Voltage Rejection Ratio	5 (typ)	5 (typ)	mV/V
Neg Supply Voltage Rejection Ratio	10 (typ)	10 (typ)	mV/V
Neg Supply Current	7.0	7.0	mA
Power Consumption	170	170	mW
Average TC of Input Offset Current	2.0 (typ)	2.0 (typ)	nA/°C
Frequency Response (typ) −3 dB Bandwidth	3.0 (typ)	3.0 (typ)	MHz
3° Relative Phase Shift	750 (typ)	750 (typ)	kHz
1% Absolute Error Due to Input-Output Phase Shift	30 (typ)	30 (typ)	kHz

*Parameters apply over operating temperature range and are min/max limits unless otherwise specified.

[1] f = 20 Hz

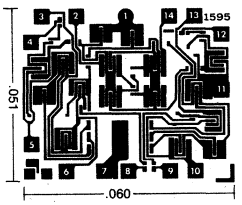
[2] Voltage applied between pins 2-1, 14-1, 1-9, 1-12, 1-4, 1-8, 12-7, 9-7, 8-7, 4-7.

Multiply with Op Amp Level Shift

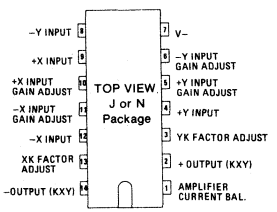


SET UP	RESISTOR* / TOLERANCE	R_1 5%	R_5 1%	R_6 1%	R_7 1%	R_8 1%	R_9 1%	R_{13} 1%	R_A 5%	R_B 20%	R_L 0.5%	R_X 5%	R_Y 5%
1	V^+ = +32 V, V^- = −15 V −10 V ≤ V_x ≤ +10 V −10 V ≤ V_y ≤ +10 V	9.1	121	100	11	121	15	13.7	12	5.0	11	15	15
2	V^+ = +15 V, V^- = −15 V −5 V ≤ V_x ≤ +5 V −5 V ≤ V_y ≤ +5 V	3.0	300	100	100	300		13.7	12	5.0	3.4	8.2	8.2
3	V^+ = +15 V, V^- = −15 V −10 V ≤ V_x ≤ +10 V −10 V ≤ V_y ≤ +10 V	1.2	121	100	11	910	13.7	13.7	12	5.0	1.5	15	15

* All resistors are k ohms.



SG1595/1495 Chip (See D-package diagram for pad functions)



CONNECTION DIAGRAM

SG1596/1496

The SG1596/1496 are monolithic double-balanced modulator/demodulator devices designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include modulation and demodulation of AM, SSB, DSB, FSK, FM and phase encoded signals. Additional uses include frequency doubling, linear mixing and chopping.

- **Excellent carrier suppression**
- **Fully balanced inputs and output**
- **Low offsets and drift**
- **High common mode rejection**
- **Adjustable gain and signal handling**
- **Useful to 100MHz**

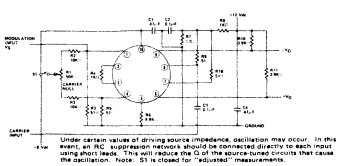
PARAMETERS/CONDITIONS*	1596	1496	UNITS
Operating Temperature Range	−55 to +125	0 to +70	°C
Applied Voltage[1]	30	30	V
Differential Input Signal, ($V_7 - V_8$)	±5.0	±5.0	V
Differential Input Signal, ($V_4 - V_1$)	±(5 + I_5 R_e)		V
Input Signal, ($V_2 - V_1$, $V_3 - V_4$)	5.0	5.0	V
Package Types	J, T	J, T, N	−−
Carrier Feedthrough			
v_c = 60 mV(rms) sine wave, f_c = 1.0kHz, offset adjusted (typ)	40	40	μVrms
v_c = 60 mV(rms) sine wave, f_c = 10MHz, offset adjusted (typ)	140	140	
v_c = 300 mV_{pp} square wave, f_c = 1.0kHz, offset adjusted (max)	0.2	0.4	
v_c = 300 mV_{pp} square wave, f_c = 1.0kHz, offset not adjusted (max)	100	200	
Carrier Suppression			
f_s = 10kHz, 300 mV(rms), f_c = 500kHz, 60 mV(rms) sine wave offset adjusted (min)	50	40	dB
f_s = 10kHz, 300 mV(rms), f_c = 10MHz, 60 mV(rms) sine wave offset adjusted (typ)	50	50	
Transadmittance Bandwidth			
R_L = 50Ω, Carrier Input Port, v_c = 60 mV(rms) sine wave, f_s = 1.0kHz, 300 mV(rms) sine wave	300 (typ)	300 (typ)	MHz
Signal Input Port, v_s = 300 mV(rms) sine wave[2]	80 (typ)	80 (typ)	
Voltage Gain, Signal Channel v_s = 100 mV(rms), f = 1.0kHz[2]	2.5	2.5	V/V
Input Resistance, Signal Port f = 5.0MHz[2]	200 (typ)	200 (typ)	kΩ
Input Capacitance, Signal Port f = 5.0MHz[2]	2.0 (typ)	2.0 (typ)	pF
Single Ended Output Resistance f = 10MHz	40 (typ)	40 (typ)	kΩ
Single Ended Output Capacitance, f = 10MHz	5.0 (typ)	5.0 (typ)	pF
Input Bias Current ($I_1 + I_4$)/2 or ($I_7 + I_8$)/2	25	30	μA
Input Offset Current ($I_1 - I_4$) or ($I_7 - I_8$)	5.0	7.0	μA
Average TC of Input Offset Current	2.0 (typ)	2.0 (typ)	nA/°C
Output Offset Current ($I_6 - I_9$)	50	80	μA
Average TC of Output Offset Current	90 (typ)	90 (typ)	nA/°C
Signal Port Common Mode Input Voltage Range f_s = 1.0kHz	5.0 (typ)	5.0 (typ)	V_{p-p}
Signal Port Common Mode Rejection Ratio[2]	−85 (typ)	−85 (typ)	dB
Common Mode Quiescent Output Voltage	8.0 (typ)	8.0 (typ)	V
Differential Output Swing Capability	8.0 (typ)	8.0 (typ)	V_{p-p}
Positive Supply Current ($I_6 + I_9$)	3.0	4.0	μA
Negative Supply Current (I_{10})	4.0	5.0	mA
Power Dissipation	33 (typ)	33 (typ)	mW

*Parameters are for T_A = 25°C and are min/max limits unless otherwise specified.

[1] Voltage applied between pins 6—7, 8—1, 9—7, 9—8, 7—4, 7—1, 8—4, 6—8, 2—5 and 3—5.

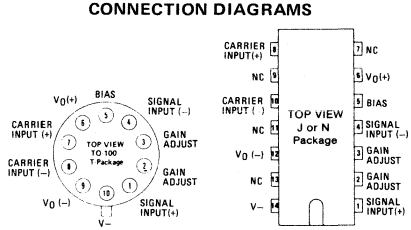
[2] $V_7 - V_8$ = 0.5 Vdc

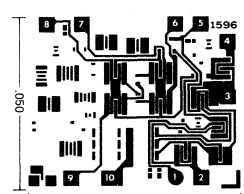
TYPICAL MODULATOR CIRCUIT



Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation. Note: S1 is closed for "adjusted" measurements.

CONNECTION DIAGRAMS





SG1596/1496 Chip (See J-package diagram for pad functions)

SG3001T

Description

The SG3001T High Frequency Video amplifier is designed for broad-band operation to 30 MHz. This monolithic integrated circuit features differential inputs and outputs, a voltage gain of 19 dB and AGC capability of 60 dB. The SG3001T is designed for operation over the full military temperature range of -55°C to +125°C and is packaged in a 12-pin TO-5 style hermetic package.

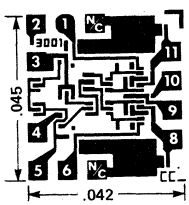
Features

- **Full differential operation**
- **150 kΩ input impedance**
- **45 Ω output impedance**
- **30 MHz bandwidth**
- **19 dB voltage gain**

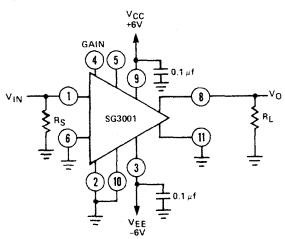
Absolute Maximum Ratings

Positive Supply Voltage	10V
Negative Supply Voltage	−10V
Differential Input Voltage	±2.5V
Common Mode Input Voltage	±2.5V
Output Current	25 mA
Power Dissipation	450 mW
Derate above +85°C	5 mW/°C
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C

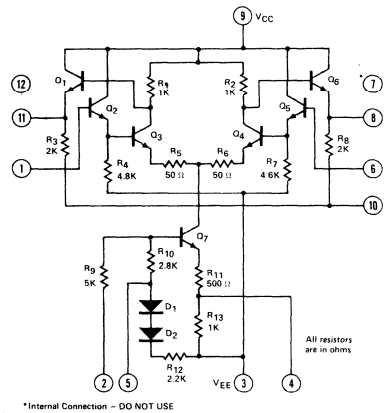
CHIP LAYOUT



CONNECTION DIAGRAM



SCHEMATIC



*Internal Connection – DO NOT USE

Electrical Characteristics (T_A = 25°C, V_{CC} = +6V, V_{EE} = -6V, f = 1.75 MHz, R_L = 1 MΩ)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		–	1.5	–	mV
Input Offset Current		–	1	10	µA
Input Bias Current		–	16	36	µA
Output Offset Voltage	R_S = 1 kΩ	–	54	300	mV
Quiescent Output Voltage	Pins 4 and 5 open	3.8	4.4	5.0	V
	Pin 5 to $-V_{EE}$	–	4.8	–	V
	Pin 4 to $-V_{EE}$	–	2.7	–	V
Quiescent Power Dissipation	Pins 4 and 5 open	60	78	120	mW
	Pin 5 to $-V_{EE}$	–	71	–	mW
	Pin 4 to $-V_{EE}$	–	110	–	mW
Differential Voltage Gain		16	19	–	dB
	f = 20 MHz	10	14	–	dB
3 dB Bandwidth	R_S = 50 Ω	16	30		MHz
Maximum Output Swing	R_S = 50 Ω	–	5	–	V_{p-p}
Noise Figure	R_S = 1k	–	5	–	dB
Common Mode Rejection Ratio	f = 1 kHz	–	88	–	dB
Input Impedance		–	150	–	kΩ
Input Capacitance		–	3.4	–	pf
Output Resistance		–	45	–	Ω
AGC Range		55	60	–	dB

Zero Voltage Switch

SG3058 / SG3059 / SG3079

Description

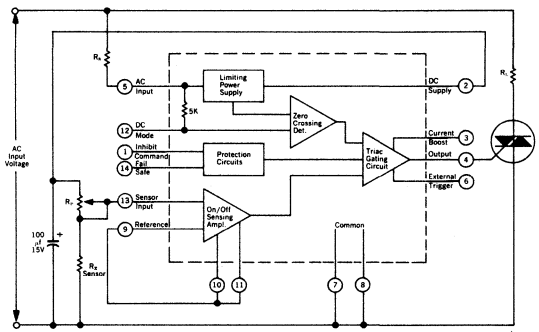
The SG3058, SG3059 and SG3079 zero crossing switching circuits are designed for a wide variety of AC power applications. These devices will operate with AC input voltages of 24 to 277 volts at frequencies of 50 to 400 Hertz and will provide an output capable of controlling most common triacs and thyristors. Each circuit contains a limiting power supply, a differential sensing amplifier, a zero-crossing detector and a triac gating circuit. The SG3058 and SG3059 additionally contain protective circuits to inhibit thyristor firing under abnormal conditions. The SG3058 is specified over the full military temperature range of −55°C to +125°C while the SG3059 and SG3079 are designed for −40°C to +85°C applications.

Features

- **24V, 120V, 220V, 277V operation at 50, 60 or 400 Hz**
- **Built-in power supply**
- **High-gain differential sensing amplifier**
- **Output synchronized with zero crossing for minimum R.F.I.**
- **150 mA output pulse current**

Absolute Maximum Ratings

DC Supply Voltage (between pins 2 & 7)	
SG3058, SG3059	14 V
SG3079	10 V
Peak Supply Current (between pins 5 & 7)	±50 mA
Output Pulse Current (pin 4)	150 mA
Power Dissipation	
J Package (cerdip) SG3058J	1000 mW
Derate above 25°C	6.7 mW/°C
N Package (plastic) SG3059N/SG3079N	600 mW
Derate above 25°C	6.0 mW/°C
Operating Temperature Range	
SG3058J	−55°C to +125°C
SG3059N, SG3079N	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering 60 sec.)	+300°C



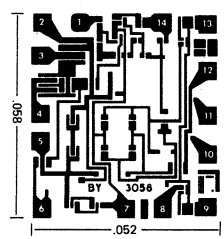
Note: Pins 12, 1, 14 and 6 are not specified for operation in SG3079 See table for value of R_s $R_p \approx R_x$. Range = 2 to 100KΩ for SG3058 and SG3059, = 2 to 50KΩ for SG3079

Electrical Characteristics (T_A = 25°C, AC Line Voltage = 120 Vrms, 50-60 Hz unless otherwise specified)

Parameter	Conditions	Limits Min.	Typ.	Max.	Units
DC Supply Voltage:					
Inhibit Mode					
@ 50/60 Hz	R_x = 10k, I_L = 0	6.1	6.5	7.0	V
@ 400 Hz	R_x = 10k, I_L = 0	—	6.8	—	V
@ 50/60 Hz	R_x = 5k, I_L = 2mA	—	6.4	—	V
Pulse Mode					
@ 50/60 Hz	R_x = 10k, I_L = 0	6.0	6.4	7.0	V
@ 400 Hz	R_x = 10k, I_L = 0	—	6.7	—	V
@ 50/60 Hz	R_x = 5k, I_L = 2mA	—	6.3	—	V
@ 50/60 Hz, SG3058	R_x = 10k, I_L = 0, T_A = −55°C to +125°C	5.5	—	7.5	V
Peak Output Pulse Current	Pin 3 open, V_{GT} = 0	50	84	—	mA
	Pin 3 & 2 connected, V_{GT} = 0	90	124	—	mA
Inhibit Input Ratio: All Types	Pin 9 to 2 Voltage Ratio	.465	.485	.520	—
SG3058	T_A = −55°C to +125°C	.450	—	.520	—
Total Gate Pulse Duration:					
Positive $\frac{dv}{dt}$ 50-60 Hz		70	100	140	μs
Positive $\frac{dv}{dt}$ 400 Hz		—	12	—	μs
Negative $\frac{dv}{dt}$ 50-60 Hz		70	100	140	μs
Negative $\frac{dv}{dt}$ 400 Hz		—	10	—	μs
Output Leakage Current: All Types		—	.001	10	μA
SG3058	T_A = −55°C to +125°C	—	—	20	μA
Input Bias Current: SG3058, SG3059		—	220	1000	nA
SG3079		—	220	2000	nA
Common Mode Input Voltage Range	Pins 9 and 13 connected	—	1.5 to 5	—	V
Pulse Mode Sensitivity	ΔV at pin 13 to change output	—	6	—	mV

AC Input Voltage (50/60 or 400 Hz) VAC	Input Series Resistor (R_x) KΩ	Power Rating for R_x W
24	2	0.5
120	10	2.0
208/230	20	4.0
277	25	5.0

CHIP LAYOUT



Applications Data (SG3058 and SG3059 only)

1. Fail-safe protection (pin 14) — When pin 14 is connected to pin 13, a special protection circuit is activated which inhibits the output if the sensor either shorts or opens. To assure proper operation of this protection, the following conditions should be observed:
   a. Limit the output current to 2 mA with a 5K dropping resistor.
   b. Set the value of R_p and the sensor resistance, Rx, between 2K and 100K ohms.
   c. Maintain a ratio of R_x to R_p between 0.33 and 3.0 over all operating conditions.
2. Inhibit command (pin 1) — A priority inhibit command at pin 1 will eliminate any output pulse. This signal should be at least 1.2V at 10μA and is compatible with DTL or T²L logic outputs.
3. External Trigger (pin 6) — The base of the Darlington NPN output stage is brought out on pin 6 for direct control of the output. Signal requirements are the same as for pin 1.
4. DC Mode (pin 12) — Connecting pins 7 and 12 disables the zero-crossing detector and allows the flow of output current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. To avoid overloading the internal power supply, the output current should be limited to 2mA with a 5K dropping resistor.

High-Voltage Fluorescent Display Driver

SG6118

ADVANCED DATA

SG6118

Performance data described herein represent design goals.
Final device specifications are subject to change.

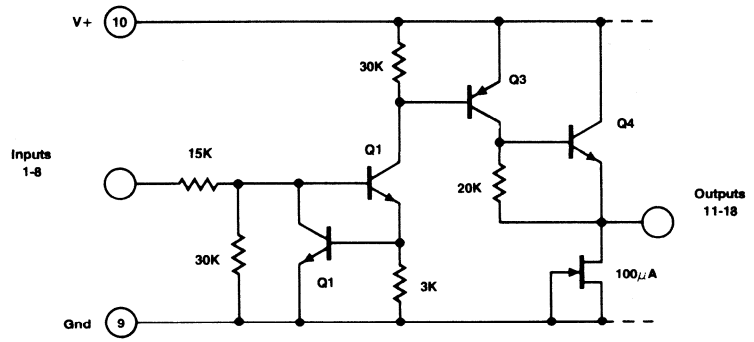
DESCRIPTION

This monolithic multiple driver IC is designed to interface between low-level digital logic and vacuum fluorescent displays. Eight independent high-voltage stages with a common bias supply are included and each output can drive either digits or segments of these displays. Each driver stage is completely self-contained with all voltage level-shifting and pull-down components incorporated within the chip. Output activation is effected when the input is pulled high.

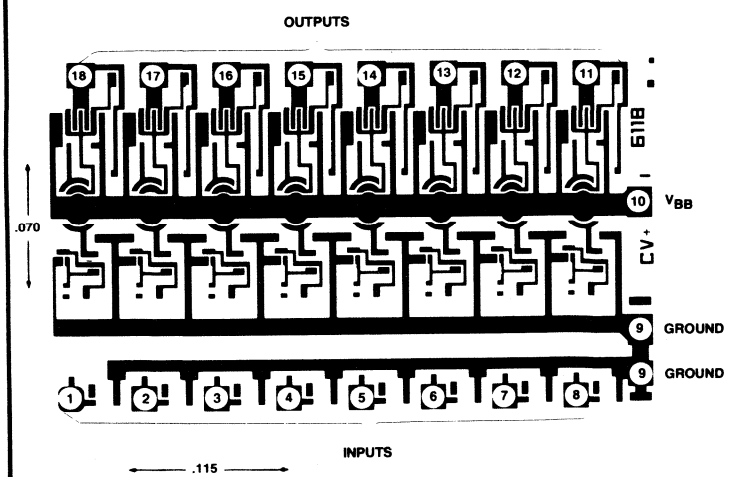
FEATURES

- **Eight independent darlington drivers**
- **Digit or segment driving capability**
- **80 volt operation with 25mA loads**
- **Integral pull-down current sinks**
- **TTL input compatibility**

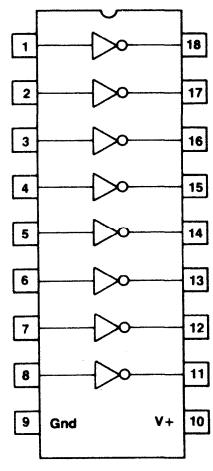
SCHEMATIC DIAGRAM (one of eight circuits shown)



CHIP LAYOUT



CONNECTION DIAGRAMS



TOP VIEW

5

High-Voltage Fluorescent Display Driver

SG6118

ADVANCED DATA
SG6118
Performance data described herein represent design goals.
Final device specifications are subject to change.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Vt	25 to 85V
Output Voltage, Vo	85V
Input Voltage, Vin	20V
Output Current, Iout	40mA
Power Dissipation, Pd	1.0W
derate above 25°C	8mW/°C

Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−55°C to +150°C

ELECTRICAL CHARACTERISTICS over operating temperature range and at Vt — 80V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Leakage Current	Vin = 0.4V	—	0.1	15	µA
Output on Voltage	Vin = 2.4V, Iout = 25mA	75	79	—	V
Pull-down Current	Input open, Vout = 80V	—	100	450	µA
Input on Voltage	Iout = 25mA	—	1.8	2.4	V
Input on Current	Vin = 5V	—	250	500	µA
Supply Current (on)	All inputs = 2.4V	—	1.1	6.0	mA
Supply Current (off)	All inputs open	—	100	225	µA

APPLICATIONS NOTES

SG1401 Video Amplifier

SG1402 Wideband Amplifier/Multiplier

SG1501A Dual Polarity Tracking Regulator

SG1524 Regulating Pulse Width Modulator

SG1543 Power Supply Output Supervisory Circuit

SG1627/1629 Dual High Current Output Driver

The SG1401-SG3401 has been designed to provide maximum versatility as a general-purpose, single-ended amplifier. With its broad frequency capability, this circuit will be useful in a wide range of applications provided that the usual considerations for high-frequency circuit designs are observed. The following information is presented toward aiding in the optimization of the many possible configurations of this device.

FIXED GAIN

In the circuit configuration shown in Figure 1, the overall voltage gain is approximated by resistors R1 and the parallel combination of R2 and R3, as

$$Av \approx 1 + \frac{R_1}{R'}, \text{ where } R = \frac{R_2 R_3}{R_2 + R_3}$$

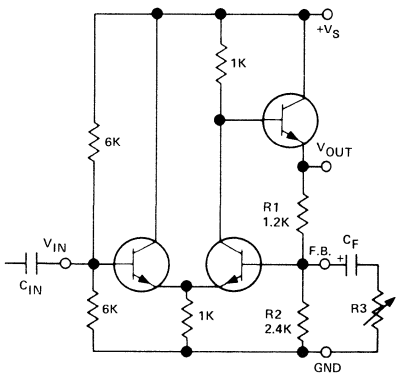


Figure 1.

With no external connections, the voltage gain is determined solely by R1 and R2 and is 1½ or 3 dB. Decreasing the effective value of R2 by capacitively coupling a lower resistor in parallel, raises the gain. Four fixed gain settings are provided internal to the circuit; however, any other setting within the maximum gain of the amplifier is possible with external resistors as shown in Figure 2.

The value of the coupling capacitor, C_F is determined by the low frequency response desired, as its capacitive reactance will add to the value of the resistance it couples. Therefore, the lower cutoff frequency will be

$$f_c \approx \frac{1}{2\pi R_3 C_F}$$

Utilizing the internal 90 or 460 ohm resistors for higher gain settings provides the added advantage of maximum temperature stability since the close tracking of adjacent diffused resistors keeps their ratio constant. Typical temperature variation of this circuit is shown below:

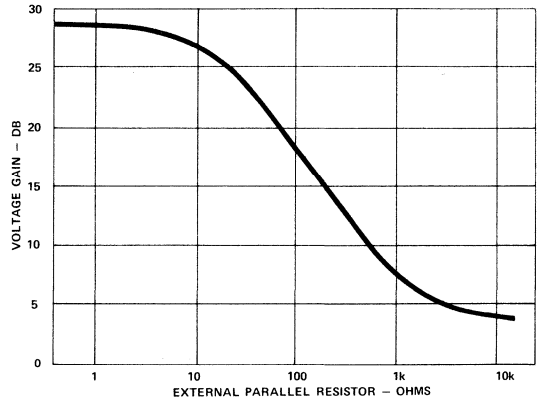


Figure 2. External Gain Control.

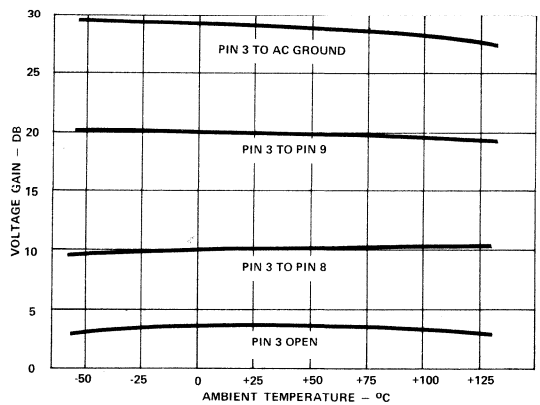


Figure 3. Temperature Stability.

VARIABLE GAIN

Since the dynamic impedance of a forward-biased diode is inversely proportional to the current through it, a convenient gain control can be achieved by using a pair of diodes as a variable impedance. In the circuit of Figure 4, R3 has been replaced by two diodes whose impedances act in parallel due to the decoupling of C_D. If the diodes are driven from a voltage source, a logarithmic relationship between gain and control signal is achieved (see Figure 5); while if a current source is used, the relationship is linear as shown in Figure 6.

There are two limitations on this form of gain control. First, the diodes' capacitance limits their effectiveness to frequencies below 20 MHz and, secondly, the signal voltage across the diodes should be held to less than 50 millivolts RMS to minimize self-modulation of amplifier gain. Additionally, the AGC current should be limited to 3 mA maximum to keep the diodes out of saturation.

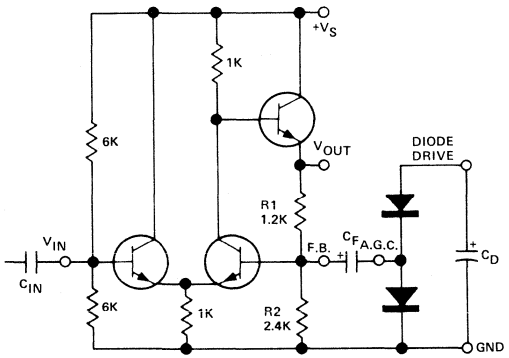


Figure 4.

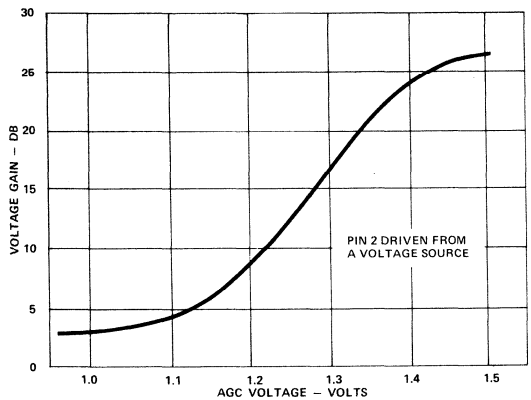


Figure 5. Gain vs. AGC Diode Voltage

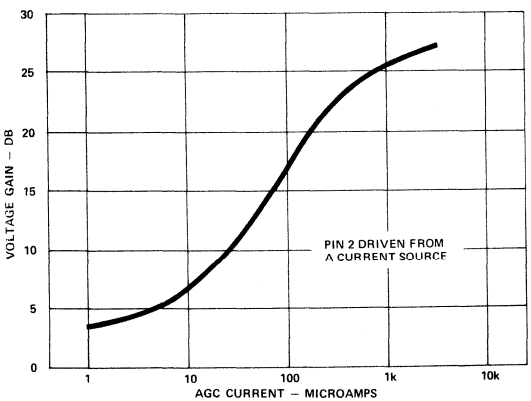


Figure 6. Gain vs. AGC Diode Current.

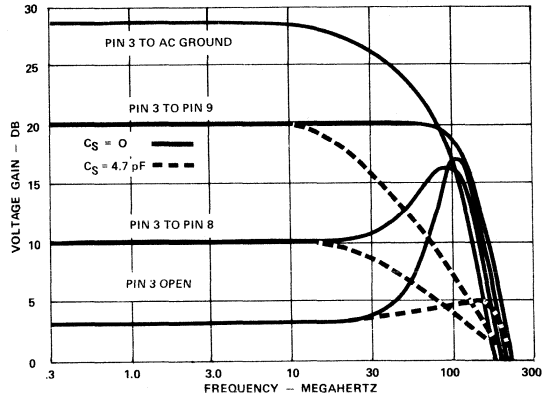


Figure 7. Frequency Response.

HIGH FREQUENCY STABILITY

With the capability of operation at 100 MHz, the SG1401-SG3401 also has some susceptibility to external stray reactances; however, with reasonable care, complete stability may be assured. Some general precautions which should be considered include the following:

(1) Power supply decoupling close to the circuit terminals (a 0.1 mfd capacitor is usually adequate).
(2) Maintain separation of input and output lines.
(3) Minimize load capacitance or insert a series resistor (up to 50 ohms) in the output.
(4) Purposely limit the high frequency response with a stabilizing capacitor C_S between pins 3 and 4.

Since the gain of this circuit is reduced by increasing the amount of feedback, the potential for instability is greatest when the gain is at its minimum value. This characteristic and the stabilizing effects of a 4.7 picofarad capacitor between pins 4 and 3 are illustrated in the frequency response curves presented in Figure 7. The relationship between the value of C_S and the upper cutoff frequency of a 20 dB gain setting is shown in Figure 8 below.

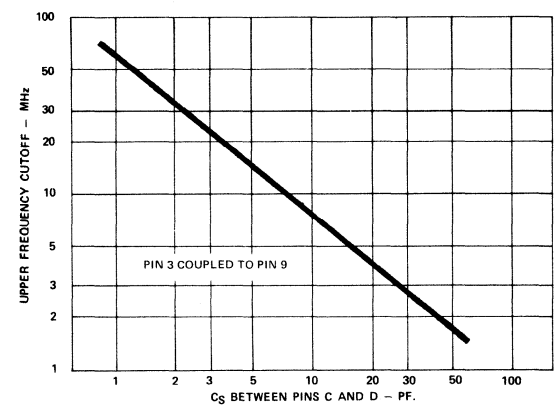


Figure 8. Upper Cutoff Frequency vs. C_S Value.

INTRODUCTION

Rapid advances in the state-of-the-art of processing monolithic linear integrated circuits have made the use of tightly matched components a practical reality. This in turn has opened the doors to a new class of circuit characterized by its utility, versatility, and ease of application. It is now possible to include on a monolithic chip, many of the components which, because of relatively poor tolerances, were formerly required to be external to the circuit. The SG1402, shown schematically in Figure 1, illustrates this capability both by its inclusion of all necessary biasing networks and by the nature of the circuit itself which requires extremely well matched component parameters for successful operation.

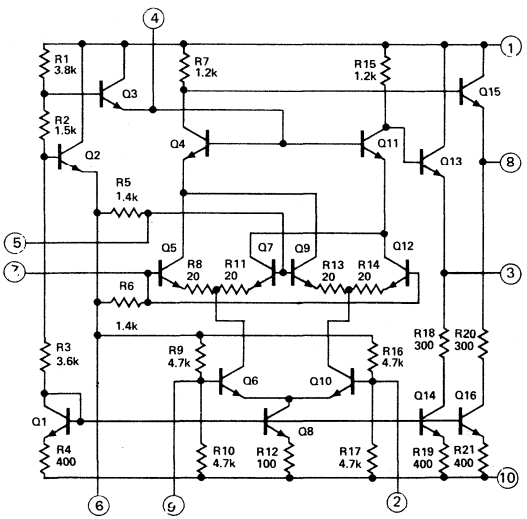


Figure 1. SG1402 Schematic Diagram.

HOW IT WORKS

The heart of the SG1402 is a four quadrant multiplier consisting of two cross-coupled differential amplifiers which are jointly controlled by a third differential amplifier. This part of the circuit is shown in simplified form as Figure 2. The constant current, I_0, is divided by Q6 and Q10 and divided again by each of the upper diff amps such that, for balanced operation, transistors Q5, Q7, Q9, and Q12 each have ¼ I_0 flowing through them. An examination of the way in which the above diff amps are cross-coupled will show that while the collector load resistors receive a portion of their current from each diff amp, the signals will arrive out of phase with respect to each other. This is because the input voltage, v_c, is amplified common emitter – with 180° phase shift – through Q9 and summed at resistor R7 with the signal which has gone common collector-common base – with 0° phase shift – through Q7 and Q5. Therefore, with the circuit perfectly balanced, the two signals completely cancel out and the output has zero signal. This can be shown mathematically as follows:

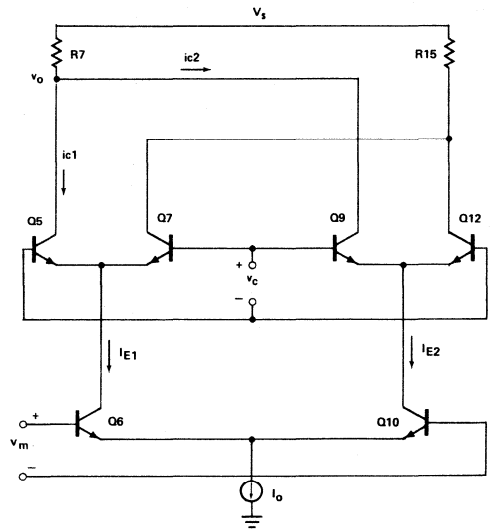


Figure 2. Simplified Schematic of the Multiplier Section of the SG1402.

The collector current in one side of a simple differential amplifier (Q5 and Q7, for example) is:

$$i_{c1} = \frac{I_{E1}}{1 + \exp\left(\frac{q}{kT} v_c\right)}$$

where: I_{E1} = sum of currents in each collector

$\frac{kT}{q}$ = 26 millivolts at 25°C

v_c = differential input voltage

This equation can be differentiated to obtain the transconductance which, for small values of v_c, is:

$$gm = \frac{di_{c1}}{d\,v_c} = \frac{q\,I_{E1}}{4kT}$$

In a similar manner, the transconductance through Q9 is:

$$gm = \frac{di_{c2}}{d\,v_c} = \frac{q\,I_{E2}}{4kT}$$

and the total voltage gain, Av is:

$$Av = R_L \frac{di_{c1}}{d\,v_c} + \frac{di_{c2}}{d\,v_c}$$

$$= \frac{R_L\,q}{4kT}\,(I_{E2} - I_{E1})$$

Since $I_{E1} + I_{E2} = I_0$, it can be seen that when $v_m = 0$, $I_{E1} = I_{E2} = \frac{1}{2} I_0$ and Av = 0. With I_{E1} and I_{E2} being collector currents of another differential amplifier, the total small-signal gain equation may be written:

$$Av = \frac{v_0}{v_c} = \frac{R_L I_0 q}{4\ kT}\left[\frac{1}{1 + \exp\left(\frac{q}{kT} v_m\right)} - \frac{1}{1 + \exp\left(\frac{q}{-kT} v_m\right)}\right]$$

The circuit gain of the SG1402 is less than that predicted by the above equation due to the local feedback offered by the 20 ohm emitter resistors. The actual relationship between Av and v_m is shown in Figure 3 while Figure 4 graphs the full four-quadrant transfer function between the input voltage, v_c, the control voltage, v_m, and the output voltage. Note that the 20 ohm emitter resistors provide linearity for ±60 millivolts of input voltage while the modulating voltage is only linear for approximately half that value. It should be recognized from Figure 4 that output limiting occurs at a constant input voltage regardless of the modulating voltage. In other words, reducing the gain reduces the maximum peak-to-peak output swing.

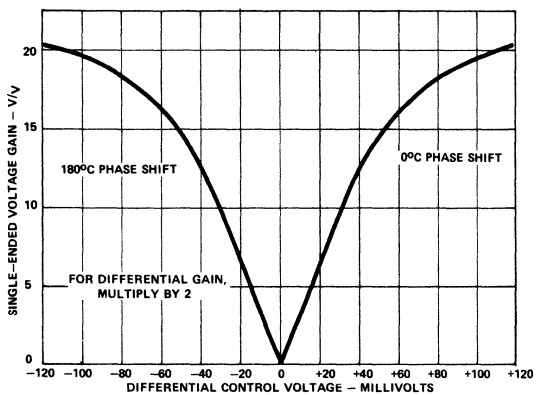


Figure 3. Differential Gain Control.

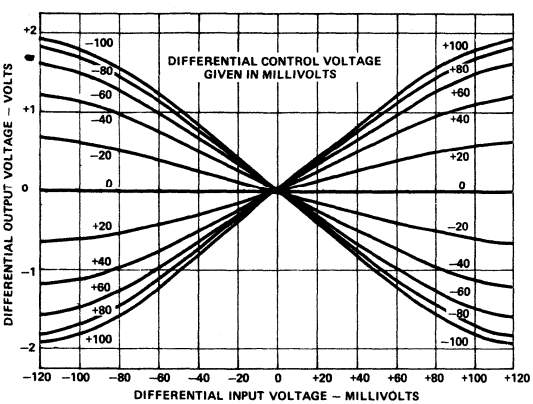


Figure 4. Multiplier Transfer Function.

BIASING CIRCUITRY

Key to the utility of the SG1402 is the inclusion of all the biasing and level shifting circuitry normally required as external components. This is provided by matched current sources and low impedance voltage sources.

Resistors R1, R2, R3 and R4 are directly across the supply voltage and establish a current:

$$I_b = \frac{V_S - V_{BEQ1}}{R1 + R2 + R3 + R4} = 1\ \text{mA at 10 volts}$$

Transistors Q14 and Q16 have the same geometries and emitter resistors as Q1 and therefore, with the same base voltage, they each are also conducting one milliamp and provide the loads for the output emitter followers, Q13 and Q15. This saves chip area as a transistor requires less space than a resistor which would establish the same current.

Transistor Q8 has four times the emitter area and ¼ the emitter resistor as Q1 and thus defines a current level I_0 of 4 milliamps.

The bias voltage levels required at different points in the circuit are all defined by the same resistors which set the current levels but there is no mutual interaction due to the insertion of Q2 and Q3 which act as low-impedance isolators.

Transistors Q4 and Q11 serve only as common-base stages to isolate the load resistor from the collector capacitance of the parallel diff-amp transistors. Thus, frequency response is improved with only slight increase in circuit complexity.

The chip layout of the SG1402 was done to optimize the component matching regardless of mask registration and process variations. From the photomicrograph shown in Figure 5, it can be seen how the symmetrical nature of the circuit was exploited to obtain matched parameters. The chip has an area of 48 by 39 mils.

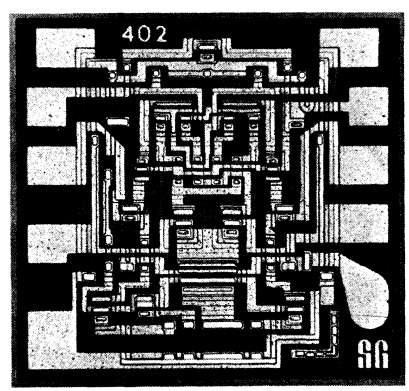


Figure 5. Photomicrograph of SG1402 Chip.

6

VARIABLE GAIN AMPLIFICATION

The circuit of Figure 6 shows the simplest application of the SG1402 as a single-ended, variable-gain amplifier. The signals at the two outputs are always equal in magnitude and opposite in phase. As the gain control potentiometer is moved from one end to the other, each output will start with a maximum signal, reduce to a minimum when the pot is centered, and increase to maximum again in the opposite phase as the wiper gets to the other end of the potentiometer.

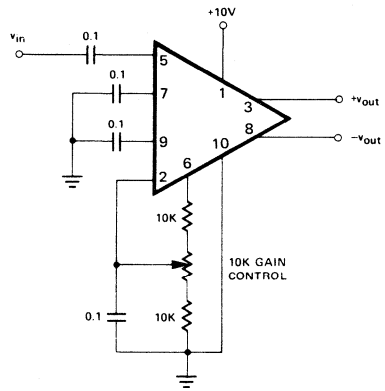


Figure 6. Single-Ended Variable-Gain Amplifier Configuration with Manual Gain Control to Provide Maximum Output of Either Phase.

For applications where a phase change is not desired, the incorporation of a diode as shown in Figure 7 will allow a DC control voltage to vary the input-output transfer function from a gain of +25 dB to an attenuation of −25 dB. This relationship is plotted in the graph of Figure 8.

Since this change in transfer function is accomplished with no net change in either operating currents or bias levels, it is transient-free and extremely fast-reacting. Thus, the circuit of Figure 7 may also be used as a gated amplifier with the control requirements compatible with 0 to 5 volt logic levels. The waveform in Figure 9 shows a 1 MHz signal controlled with a 10 microsecond pulse.

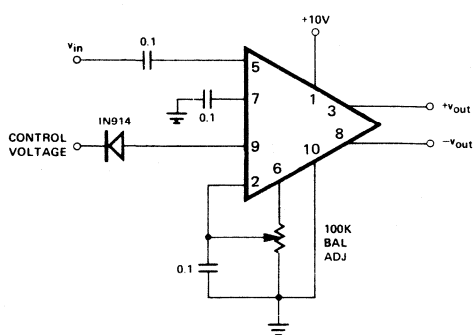


Figure 7. Addition of Diode Provides Gain Control Without Phase Change. Balance May be Eliminated if Maximum Attenuation is not Required.

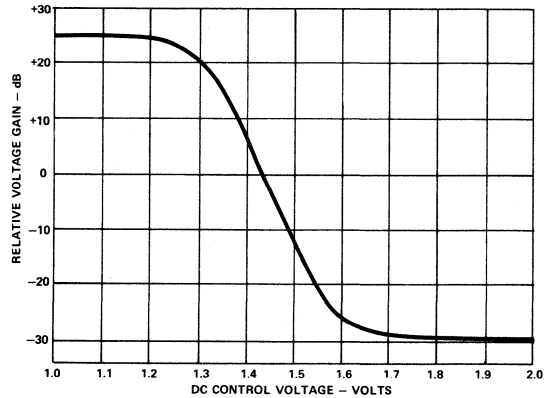


Figure 8. Gain Variation as a Function of Control Voltage with Diode Coupled Input.

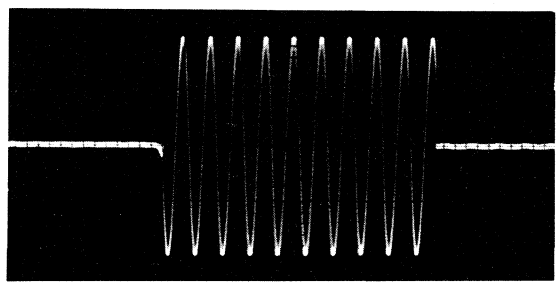


Figure 9. Gate Amplifier or Pulse Modulator Response. Input is 10 mVrms, 1 MHz and Control Voltage is 0 to 5 Volt Square Wave with f = 50 kHz.

MODULATION

The multiplying function of the SG1402 can be used to provide both balanced and amplitude modulation utilizing the basic circuit shown in Figure 10. With the potentiometer adjusted for optimum balance, the carrier signal is canceled out producing a doublesideband waveform at the output. Depending upon the amplitude of the carrier signal, higher frequency harmonics can also be generated; however, if only the lower sideband is used, filtering of the upper sideband will also eliminate all the harmonics. It should be noted that this balanced modulation is achieved without the need for the usual transformers and only capacitive coupling is required. Typical waveforms are shown in Figure 11.

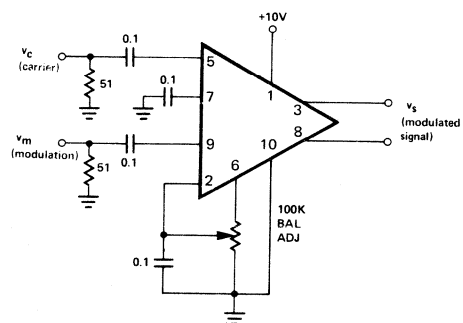


Figure 10. Balanced Modulator.

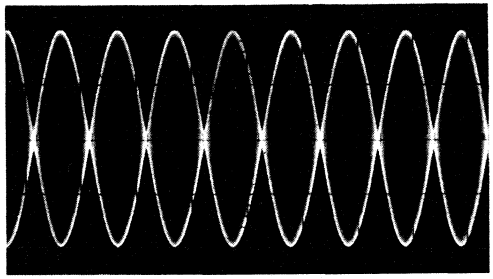


Figure 11. Balanced Modulator Output Waveform. (0.1V/cm, 50 μs/cm, f_c = 1 MHz, f_m = 10 KHz).

If the potentiometer is adjusted so that the circuit is unbalanced, then the carrier is included in the output signal and amplitude modulation as shown in Figure 12 results. The optimum adjustment can most readily be made while observing the output waveform on an oscilloscope. Care should be taken that neither signal overdrive the circuit.

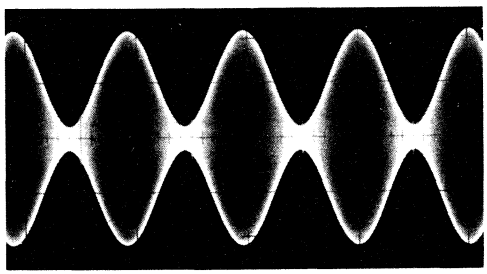


Figure 12. Amplitude Modulator Output Waveform. (0.2V/cm, 50 μs/div, f_c = 1 MHz, f_m = 10 KHz).

By using a signal to modulate itself with the circuit shown in Figure 13, the input is squared and since

$$\cos^2 \omega t = \tfrac{1}{2} [1 + \cos 2 \omega t]$$

the output frequency is twice that of the input. Typical waveforms for this frequency doubler application are shown in Figure 14.

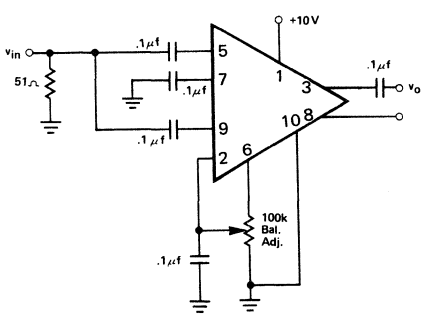


Figure 13. Frequency Doubler.

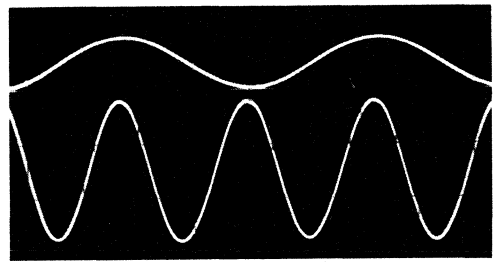


Figure 14. Frequency Doubler Input and Output Waveform. (50mV/cm, 0.2 μs/div, f_1 = 1 MHz, f_2 = 2 MHz).

DEMODULATORS

The same features which make the SG1402 an excellent modulator provide superior performance when the circuit is used as a single or double sideband demodulator. The circuit of Figure 15 illustrates the simplicity of this application. The balance pot is not necessary since the inserted carrier is eliminated by the low-pass filter at the output.

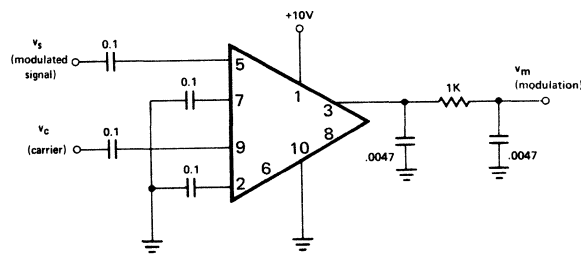


Figure 15. Balanced Demodulator.

The same general approach may be used for amplitude modulation and a block diagram of a simple AM detector is shown in Figure 16. Thus, the SG1402 can be used in receivers which combine SSB and AM to provide complete signal transformation in either mode of operation.

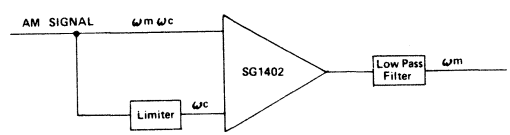


Figure 16. AM Detector Block Diagram.

CONCLUSIONS

With the introduction of the SG1402, Silicon General has provided a powerful tool to the communications engineer and all others working with information processing. Because of its versatility and capability, this device opens the way to a much greater utilization of carrier transmission schemes for data handling in applications ranging from outer space to home kitchens.

CIRCUIT OPERATION

The first IC to combine a positive and negative voltage regulator on a single chip was the SG1501, and this device has since been supplemented with three new tracking regulator designs – the SG1502, the SG1501A, and the SG1568.

All four of these tracking regulators operate in a similar manner which is best visualized through the block diagram shown in Figure 1. This circuit is fundamentally a tracking regulator. That is, the negative voltage is regulated and the positive output tracks the negative. (Note: In the SG1568, the circuit is reversed in that the negative side tracks the regulated positive output; however, the principle is the same.) Negative regulation is accomplished by providing a constant-voltage reference for the negative error amplifier, but the reference input to the positive error amplifier is grounded. This amplifier forces its other input, which is the center-tap between equal resistors, to also be at zero volts, thus requiring the positive output to be equal in magnitude but opposite in polarity to the negative output.

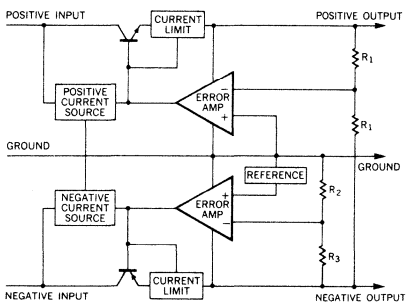


Figure 1. Block Diagram

With this technique, a single adjustment of the negative voltage divider – which changes the negative output level – will also provide exactly the same change to the positive output voltage. This tracking will hold all the way from approximately one volt above the reference voltage to a maximum value of about two volts less than the input supply voltage.

DESIGNER'S CHOICE

With four IC's to choose from some discussion of the significant features of each type is in order. Three of the devices, the SG1501A, the SG1501 and the SG1568 are factory set at ±15V regulators while the fourth, the SG1502, is user-adjusted to provide outputs from ±8V to ±28V.

The SG1501 and SG1501A are interchangeable and both can be used by themselves to provide load currents to the maximum defined by package dissipation, or can be combined with external pass transistors for currents in excess of two amps. Both devices feature constant current limiting with the value set by an external resistor. The SG1568 is similar in all respects to the SG1501 except that it is frequency compensated in a slightly different way.

The SG1502 uses the same basic circuit as the SG1501 but has two important differences. First, the voltage setting resistors are external to the device providing greater flexibility in adjusting the output voltage levels to other than ±15V. Secondly, the current limit circuitry has been changed to allow its use in a foldback mode. Foldback current limiting provides for a short circuit current value less than the maximum load current and is a significant feature when the major power dissipation is in external pass transistors rather than the IC.

Self-contained thermal shutdown is the primary improvement offered by the SG1501A although increases in both the maximum input voltage and load current have also been made. With thermal shutdown, temperature sensing circuitry on the chip is designed to turn off the output current when the junction temperature exceeds a safe limit – typically 170°C. The significance of this feature is that the designer now need not design around short-circuit power dissipation limits – the device will take care of itself. Since short-circuit power is typically more than twice as much as maximum operating power, this means a two-times, or better, improvement in load current is possible. It should be noted that even with thermal limiting circuitry, the maximum current must be controlled to allow time for this protection to react.

APPLICATIONS

The simplest way to use the SG1501 and SG1501A is in the basic circuit shown in Figure 2. In this form, the device will handle 50 to 100 mA, depending on the heat sinking (more about this later) and will provide ±15V outputs with typically less than two millivolts of sensitivity to either line or load variations. Because of this excellent line regulation, there is no need for symmetrical input supply voltage levels. The only requirement is that each level be greater than its associated output and that the total voltage between positive and negative supplies be less than 60V (70V for the SG1501A). The minimum input voltage is defined by the regulator dropout characteristics shown in Figure 3.

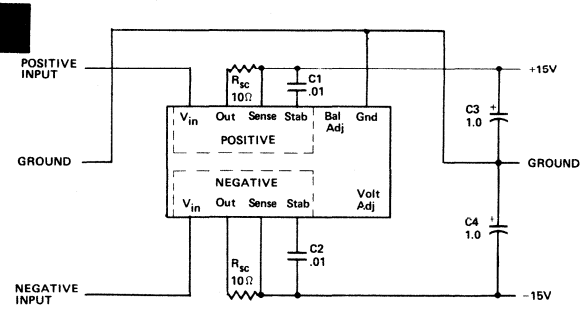


Figure 2. Basic ±15V, 50 mA Regulator

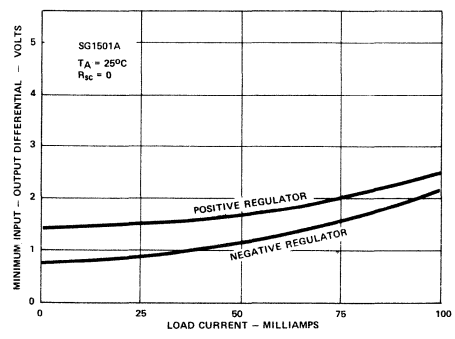


Figure 3. Regulator Dropout Voltage

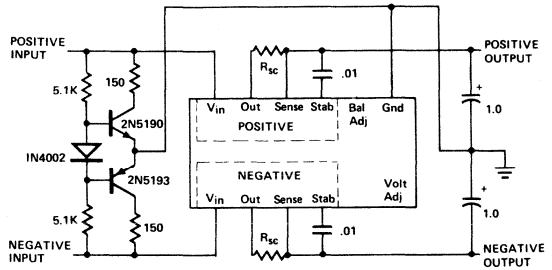


Figure 4. Artificial ground for use with an ungrounded or single level voltage.

When operating from a single voltage source, an ungrounded supply is equired. An artificial ground can be provided as shown in Figure 4. In this ircuit, the external transistors will conduct as necessary to accommodate nbalanced load requirements and while the outputs will float between the wo input levels, they will be held constant with respect to this artificial round.

URRENT LIMITING

Current sensing is provided by transistors Q12 and Q13 (see schematic, igure 5) which are normally held off by an external base-to-emitter esistor, Rsc. When the load current passing through this resistor develops nough voltage, the transistor turns on and diverts drive current away from he series pass transistors. The sense voltage is equal to approximately .6V at Tj = 25°C, but it is temperature dependent decreasing to 0.4V at 125°C as shown in Figure 6. Note that it is junction temperature that determines the sense level, and thus increasing the power dissipation within the circuit can lower the value at which limiting will occur. The value of the limiting resistor, Rsc, should be selected by:

$$Rsc = \frac{\text{Sense Voltage at Maximum Tj}}{\text{Allowable Short Circuit Current}}$$

where, for maximum regulation, the allowable short circuit current should be at least 20% more than the maximum expected load current.

Under some conditions, a low-level oscillation may be present on the negative side when the device goes into current limiting. Should this be a problem, it may be eliminated by by-passing Rsc with a capacitor whose value is such that the time constant, Rsc C, is equal to 10×10^{-6} second. This capacitor, as well as the output capacitors, C3 and C4, must be low ESR types such as solid tantalum.

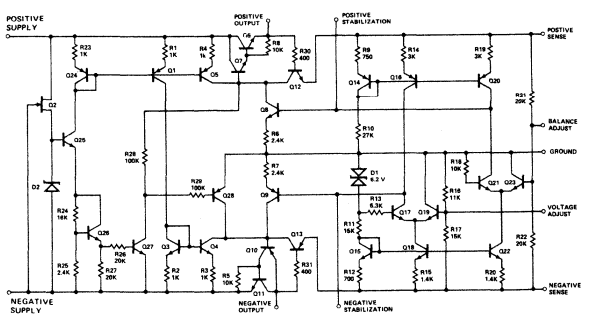


Figure 5. SG1501A Schematic Diagram

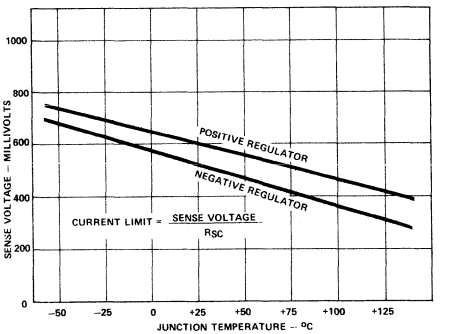


Figure 6. Current Limiting Characteristics

POWER CONSIDERATIONS

Although these dual regulators are designed to handle large load currents and high input voltages, the product of the two can easily exceed the maximum total device dissipation allowed by the package. The functional limitation which should be considered for each application is that for maximum reliability the junction temperature of the chip should not exceed 170°C. This is usually derated to give a maximum design operating Tj of 150°C.

To evaluate the maximum junction temperature possible in a given application, the following three parameters must be known:

1. The power dissipation within the chip
2. The thermal resistance from junction to ambient (or heat sink)
3. The ambient (or heat sink) temperature

The power dissipation within the chip is equal to the sum of the input voltage times the standby current plus the input-output voltage differential times the load current, for each side of the regulator. For example, the total power dissipation for ±20V inputs, ±15V outputs, and 50 mA load currents is:

$$Pd = 20\,(2) + 20\,(3) + 5\,(50) + 5\,(50)$$
$$= 100 \text{ mW standby} + 500 \text{ mW load current}$$
$$= 600 \text{ mW}$$

The thermal resistance is the resistance to heat flow from the junction to the ultimate heat sink. For parts mounted in the open, still air, the thermal resistance (θjA) is equal to 185°C/watt for the TO-100 metal can and 125°C/watt for the TO-116 ceramic DIP. Blowing air across the package, or the use of some form of heat radiator can significantly reduce these numbers. For example, the use of IERC's model TXBF-032-025B top hat radiator on the TO-100 package, reduces θjA to 130°C/watt, while their model LIC-214A-2B radiator for the TO-116 will give an θjA of 50°C/watt for that package. Finally, a perfect heat sink reduces θjA to θjC which is 50°C/watt for the TO-100 and 20°C/watt for the TO-116.

With the above information, the maximum power handling capability of the package can be determined as follows:

1. Calculate the maximum allowable junction temperature rise:

   $\Delta Tj = 150^{o}C - T_A$ (max)

2. Calculate the power availability:

   $Pd = \Delta Tj/\theta jA$

3. From this number, subtract the maximum standby dissipation:

   $Psb = (V+ \text{ max})(Isb+) + (V- \text{ max})(Isb-)$

4. The remainder can be used to determine the maximum load current as a function of input-output voltage differential.

The curves of Figure 7 show these relationships for each package under the assumptions of 25°C ambient, and symmetrical input and output voltages and load currents.

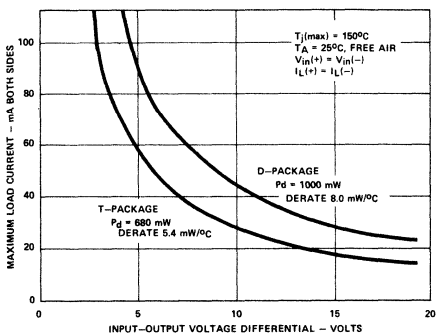


Figure 7. Maximum Current Capability

EXTERNAL POWER TRANSISTORS

Additional current handling capability may be provided through the use of external power transistors in the configuration shown in Figure 8. In this circuit, the 75 ohm base-to-emitter resistors provide a path for the regulator standby current and should not be increased in value. An additional consideration is the use of solid tantalum output capacitors as most common electrolytic types have too high an equivalent series resistance, particularly at high frequencies.

The power transistors are not critical and can be selected on the basis of current and voltage capability, and on mechanical requirements for practical heat sinking. Note that only one transistor need be used if only one side has excessive load current. Although low-frequency devices will minimize the risk of oscillation, unique transistor characteristics may require a small capacitor (0.1 mfd) from base to ground or a larger value (5 mfd) from base to emitter for complete stability.

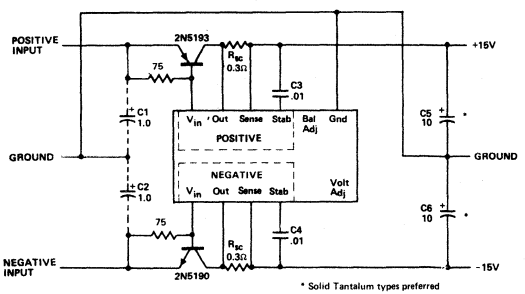


Figure 8. High Current Configuration, One Amp Output

FOLDBACK CURRENT LIMITING

With constant-current limiting as shown in Figure 8, the power dissipation in the pass transistors under short circuit conditions can be substantial. Here, the thermal limiting feature of the SG1501A can't do much good since it senses the IC temperature rather than the external transistors. To eliminate the problem of having to heat sink a short circuit power two to three times normal operating levels, the use of the SG1502 in the circuit of Figure 9 should be considered. The dividers of R5 and R6 pre-bias the current limiting such that when the output is shorted, the maximum current is substantially reduced from its normal operating level. The values for R5 and R6 are most easily determined from an itterative solution of the equations below with the trade-off being that a greater amount of foldback requires a larger voltage drop across Rsc:

$$\text{Max Load Current} \approx \frac{\text{Sense Voltage} + \frac{R5}{R6} Vo}{Rsc}$$

$$\text{Short Circuit Current} \approx \frac{\text{Sense Voltage}}{Rsc}$$

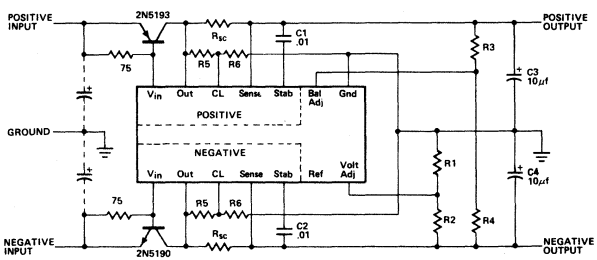


Figure 9. Foldback Current Limiting

VOLTAGE ADJUSTMENTS

With both output voltage levels internally set for 15V, (±200 mV for the SG1501/2501 and ±500 mV for the SG3501) these devices require no additional resistors for many applications. It is possible, however, to externally vary the output voltages from ±10 to ±23V by using external resistors to shunt one or both of the internal resistors which set the negative output level. The positive output will, of course, track the negative value.

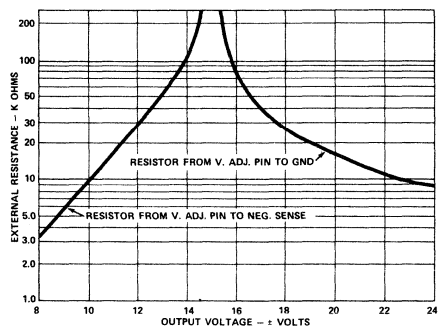


Figure 10. External parallel resistor required for voltages other than ±15V.

The simplest way of changing the output levels is to use a single resistor

in parallel with R17 (see Figure 5) for voltages less than 15V and in parallel with R16 for voltages above 15V. The graph of Figure 10 shows the approximate value to use in either case.

This method of adjusting output levels has one disadvantage, however. Diffused resistors have a positive temperature coefficient and while they can be made to track each other extremely well, with one of them shunted this tracking becomes degraded. A method offering greater temperature stability is the use of a pair of resistors with values low enough to swamp out the internal divider. By shunting R16 with 1.2k, and R17 with a resistor selected by:

$$R17'' = \frac{1.2\,(Vo - 6.2)}{6.2}\ k\Omega$$

where Vo is the desired output voltage, a four-fold improvement in temperature performance is achieved at the expense of the additional divider current. Figure 11 shows that temperature variation which may be expected both with a single shunt resistor and with a divider drawing approximately five milliamps of current. Note that these temperature shifts are caused by changes in chip temperature which could result from variations of either ambient temperature or internal power dissipation.

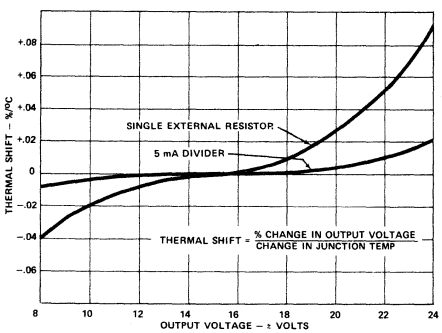


Figure 11. Temperature Coefficient of Output Voltage

In the 14 pin dual-in-line package, a connection is provided to the junction of R21 and R22. An external resistor divider can be used here in the same manner to either balance the two outputs so that they are exactly equal in magnitude or to unbalance them for non-symmetrical output levels.

Although all of these dual regulator types have provisions for adjustment of the output voltage levels, with its user-supplied voltage setting resistors, the SG1502 is the best choice for applications very far from ±15V. The divider resistors (see Figure 9) are selected as follows:

$$\text{Negative Vo} = \frac{6.2\,(R1 + R2)}{R1}$$

$$\text{Positive Vo} = \frac{R3}{R4}\,(\text{Negative Vo})$$

One common application for positive and negative voltages is as a power source for the widely used 710 and 711 IC voltage comparators. Since these devices are designed for +12 and −6V operation, it takes a circuit as shown in Figure 12 to get around the ± 8V minimum output limitation of these regulators. Here, the nominal ±15V output of the SG1501 has been reduced to ±12V by the 2.0k and 1.8k voltage divider. Six volts are then subtracted from the negative output by the IN4735 zener diode. Because the diode is outside the feedback loop, some minor variations in the −6V output may be observed due to its temperature coefficient or dynamic impedance. These variations have negligible effect on the comparators, however, as the negative voltage is used only to bias high impedance current sources.

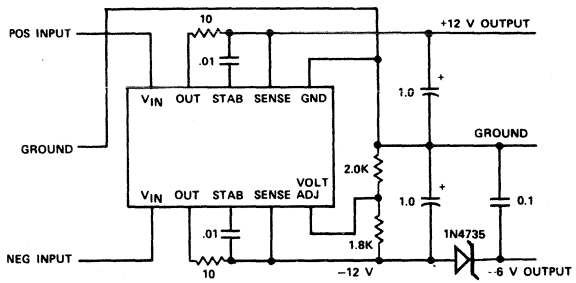


Figure 12. Using the SG1501 to provide +12 and −6V outputs.

Zener diodes can also be put to use in applications requiring high input voltages. In the circuit of Figure 13, the small signal zener diodes reduce the voltage applied to the IC while allowing the easily heat-sinked power transistors to absorb the added power dissipation caused by a large input-output differential.

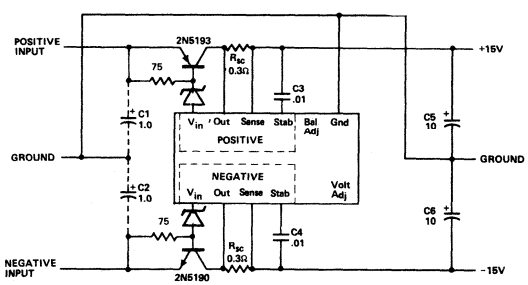


Figure 13. Zener diodes used to prevent high input voltages from appearing across the device.

CONCLUSIONS

With two complete regulators in a single IC, these new regulators offer an improved approach to power distribution. Their high degree of performance and freedom from large numbers of external components make "on-card", or distributed regulation a practical reality. By regulating at the point of use, the system designer has eliminated many knotty problems such as lead inductance, decoupling, line drop through connectors, etc. In addition, since each circuit card or module can now regulate its own voltage, complete interchangeability is more nearly assured and the problems of equipment maintenance are greatly eased.

SIMPLIFYING CONVERTER DESIGN WITH A NEW INTEGRATED REGULATING PULSE WIDTH MODULATOR

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Abstract

A new monolithic integrated circuit is described which contains all the control circuitry for a regulating power supply converter or switching regulator. Included in this 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches, and current limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformer-less voltage doublers and polarity converters, as well as other power control applications.

INTRODUCTION

Implementing a switching power supply has just become significantly easier with the introduction of the SG1524 series of Regulating Pulse Width Modulator integrated circuits. Long recognized as offering greatly improved efficiencies, the development of switching supplies has been hampered by the complexity of the low-level circuitry required to provide the proper signals for adequate control of the switching transistors. As a result, these supplies have tended to be more costly, larger in size, and with poorer reliability than could be justified by their improved efficiency. Even when threats of higher energy costs and potential brown-outs have made switching supplies mandatory, their complexity has made the engineering design task a most formidable undertaking.

With the introduction of the SG1524, a major portion of the complex low-level control circuitry has been integrated into a single LSI linear integrated circuit. This monolithic chip, packaged in a 16-pin dual-in-line outline, implements the entire block diagram shown in Figure 1.

It is the integration of all these different functions into a single IC that qualifies the SG1524 as one of the best examples to date of large scale integration as applied to analog circuits.

The remainder of this paper will describe each of the individual blocks in the following diagram in considerable detail and then offer a few basic application suggestions.

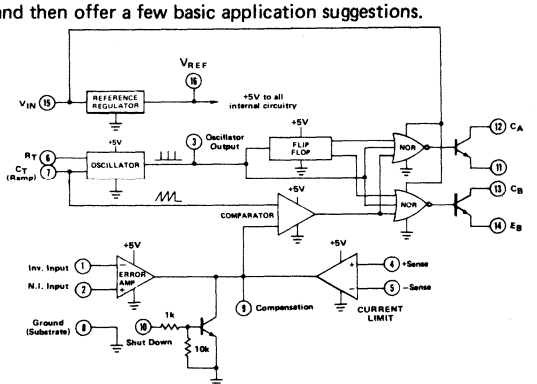


FIGURE 1 – SG1524 BLOCK DIAGRAM

VOLTAGE REFERENCE

The reference circuit of the SG1524 is shown in Figure 2. This is a complete linear regulator designed to provide a constant 5 volt output with input voltage variations of 8 to 40 volts. It is internally compensated and short circuit protected. It is used both to generate a reference voltage and as the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5 volt

source by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6 volts. While discussing input power, it should be mentioned that the entire SG1524 IC draws less than 10 mA of current, regardless of input voltage.

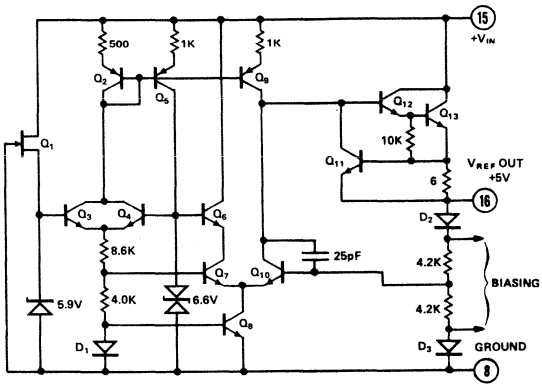


FIGURE 2 – SG1524 REFERENCE CIRCUIT

This reference regulator may be used as a 5 volt source for other circuitry. It will provide up to 50 mA of output current itself and can easily be expanded to higher currents with an external PNP transistor as shown in Figure 3.

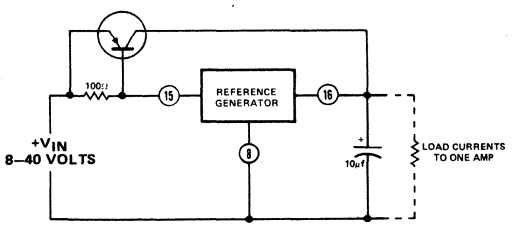


FIGURE 3 – SG1524 EXPANDED CURRENT SOURCE

OSCILLATOR

The oscillator in the SG1524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). This constant-current charging gives a linear ramp voltage which provides an overall linear relationship between error voltage and output pulse width. The SG1524 oscillator circuits is shown in Figure 4.

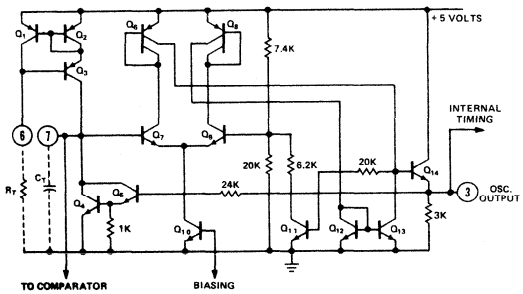


FIGURE 4 – SG1524 OSCILLATOR CIRCUIT

A second output from the oscillator is a narrow clock pulse which occurs each time C_T is discharged. This output pulse is used for several functions as outlined below:

(1) As a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. The width of this blanking pulse can be controlled to some extent by the value selected for C_T.

(2) As a trigger for an internal flip-flop which directs the PWM signal to alternate between the two outputs. Note that for single-ended applications, the two outputs can be connected in parallel and the frequency of the output is the frequency of the oscillator. For push-pull applications, the outputs are separated and the action of the flip-flop provides an output frequency ½ that of the oscillator.

(3) As a convenient place to synchronize an oscilloscope for system de-bugging and maintenance.

(4) As a bi-directional port for external timing synchronization. The output pulse from this oscillator – which is stable to within 2% over variations in both input voltage and temperature – can be used as a master clock for other circuitry, including other SG1524's. It thus follows that a positive pulse applied to this terminal can synchronize the SG1524 to an external clock signal.

The waveforms of the two outputs from the oscillator are shown in Figure 5.

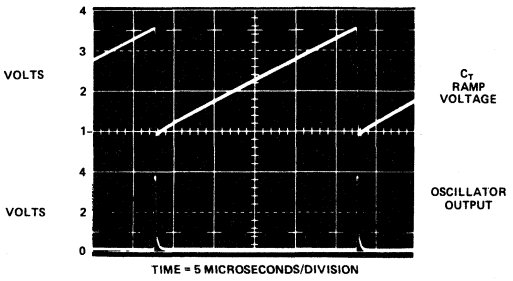


FIGURE 5 – SG1524 OSCILLATOR WAVEFORMS

ERROR AMPLIFIER

The error amplifier circuit, shown in Figure 6, is a simple differential input, transconductance amplifier. Both inputs and the

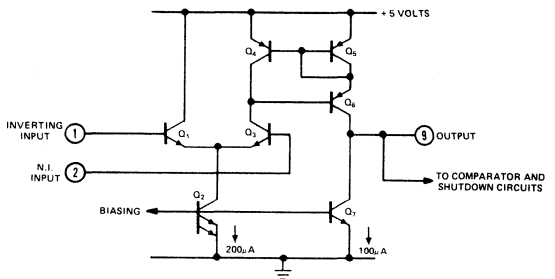


FIGURE 6 – SG1524 ERROR AMPLIFIER SCHEMATIC

output are available for maximum versatility. The gain of this amplifier is nominally 10,000 (80 dB) but can be easily reduced by either feedback or by shunting the output to ground with an external resistor. The overall frequency response of this amplifier which, by the way, is not internally compensated but yet is stable with unity gain feedback, is plotted with various values of external load resistance in Figure 7.

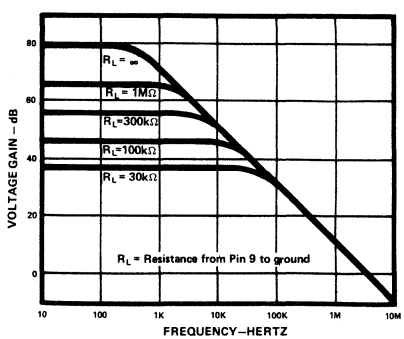


FIGURE 7 – SG1524
ERROR AMP FREQUENCY RESPONSE

Phase shifting to compensate for an output filter pole may readily be accomplished with an external series R-C combination at the output terminal of the amplifier.

Since the error amplifier is powered by the 5-volt reference voltage, the acceptable common-mode input voltage range is restricted to 1.8 to 3.4 volts. This means the reference must be divided down to be compatible with the amplifier input, but yet provides the advantage of being able to be used to regulate negative output voltages. Required input dividers are shown in Figure 8.

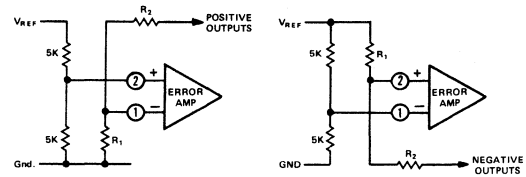


FIGURE 8 – ERROR AMPLIFIER CONNECTIONS

Since this amplifier is a transconductance design, the output is a very high impedance (approximately 5 MΩ) and can source or sink only 200 microamps. This makes the output terminal (Pin 9) a very convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200 μA can pull this point to ground, thereby shutting off both outputs.

For example, the soft start circuit of Figure 9 can be used to hold Pin 9 to ground – and thus both outputs off– when power is first applied. As the capacitor charges, the output pulse slowly increases from zero to the point where the feedback loop takes control. The diode then isolates this turn-on circuit from whatever frequency stabilizing network might also be connected to Pin 9.

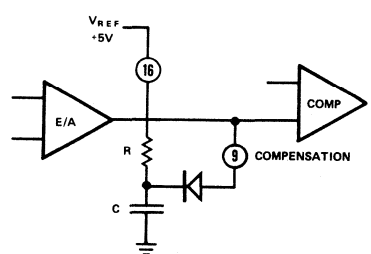


FIGURE 9 – SG1524 SOFT START CIRCUITRY

CURRENT LIMITING

The current limiting circuit, while shown in the block diagram as an op amp, is really only a single transistor amplifier as shown in Figure 10. It is frequency compensated and has a second transistor to provide temperature compensation and a reduction of input threshold to 200 mV. When this threshold

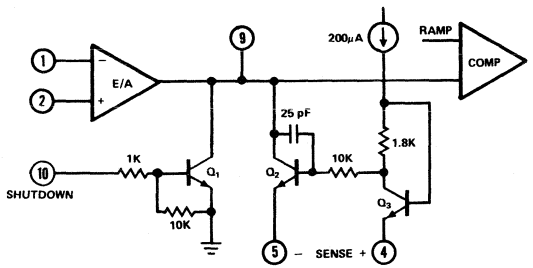


FIGURE 10 – SG1524 CURRENT LIMITING

is exceeded, the amplifying transistor turns on and, by pulling the output of the error amplifier toward ground, linearly decreases the output pulse width. One consideration in using this circuit is that the sense terminals have a ±1 volt common mode range which requires sensing in the ground line. However, since differential inputs are available, foldback current limiting can be implemented as shown in Figure 11.

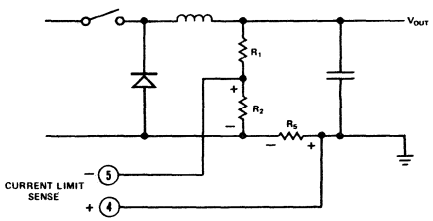


FIGURE 11 – FOLDBACK CURRENT LIMITING

While on the subject of protection circuitry, although overvoltage protection is not built into the SG1524, it is relatively easy to add by using the internal shutdown circuit in conjunction with a few external components as shown in Figure 12.

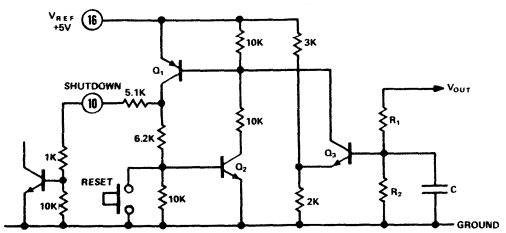


FIGURE 12 – SG1524 OVER VOLTAGE PROTECTION

This circuit will provide a low level sensing and latching function and while it won't protect against a shorted output transistor, it will remove the drive signals with no power dissipation.

OUTPUT STAGES

The outputs of the SG1524 are two identical NPN transistors with both collectors and emitters uncommitted. These circuits are as shown in Figure 13 and include an antisaturation network for fast response and current limiting set for a maximum output current of approximately 100 mA.

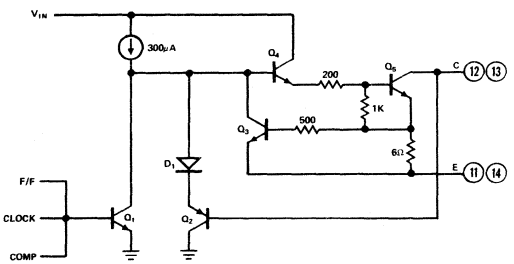


FIGURE 13 – SG1524 OUTPUT STAGE

The availability of both collectors and emitters allows maximum versatility to enable driving either NPN or PNP external transistors; however, it must be remembered that this is only a switch which closes and opens. Power transistor turn-off drive must be developed externally. Some suggestions for output drive circuits are shown in Figure 14.

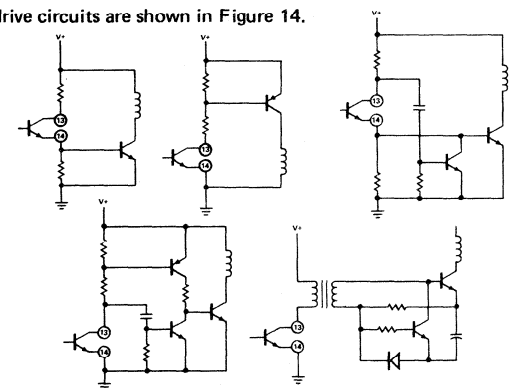


FIGURE 14 – DRIVING EXTERNAL TRANSISTORS

APPLICATIONS

In considering applications for the SG1524, it appears that there are three general classifications of switching power supply

systems. Included in the first are the transformerless voltage multiplier circuits shown in Figure 15. These circuits are primarily used for low level applications but can step up, step

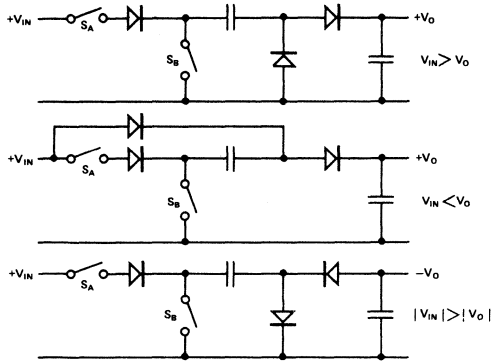


FIGURE 15 – CAPACITOR/DIODE OUTPUT CIRCUITS

down, or change the polarity of an input voltage. The switches shown can be either the output stages of the SG1524 or external transistors. Note that one extra diode is required to protect the emitter-base junction of switch S_A during the times when both switches are open.

For higher current applications, the single-ended inductor circuits of Figure 16 represent another classification. Here the two

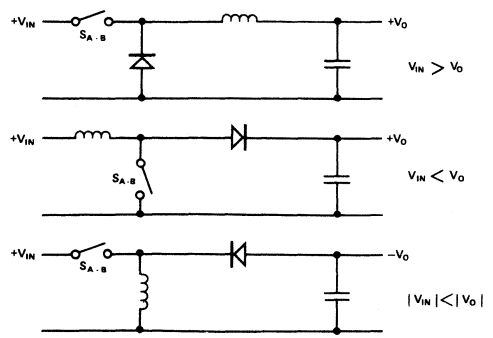


FIGURE 16 – SINGLE-ENDED INDUCTOR CIRCUITS

outputs of the SG1524 are connected in parallel, but note that this does not give twice the current as the switches are alternating internally. This does not affect external performance, however, and the SG1524 can be used to provide 0-90% duty cycle modulation in any of the configurations shown.

The third general classification of power supply systems are transformer coupled, two types of which are shown in Figure 17.

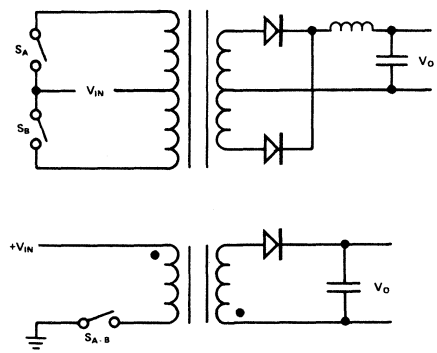


FIGURE 17 – TRANSFORMER COUPLED CIRCUITS

The push-pull circuit represents the conventional DC to DC converter with each switch being controlled for 0 - 45% duty cycle modulation. The second transformer circuit is a single-ended flyback converter, useful at light loads without a separate output inductor.

To illustrate the use of the SG1524 in each of the above general classifications, the following simple, but practical, circuits are presented:

Figure 18 shows the use of the SG1524 as a low current polarity converter providing a regulated –5 volt output at currents up to 20 mA from a single positive input voltage. The external

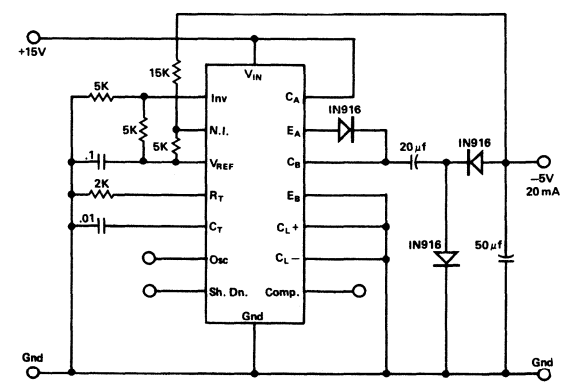


FIGURE 18 – LOW CURRENT POLARITY CONVERTER

components required include the divider resistors to interface the reference and output voltages with the error amplifier, a resistor/capacitor to set the operating frequency, and the output diodes and capacitors. The combination of the built-in current limiting of the SG1524 output stages and the capacitor

coupling of the output signal provide full protection against short circuits and the current limit amplifier is unused. Since this circuit has no inductor, the output capacitor is more than enough to stabilize the regulating loop and no additional compensation is required.

Another low-level circuit is the flyback converter shown in Figure 19.

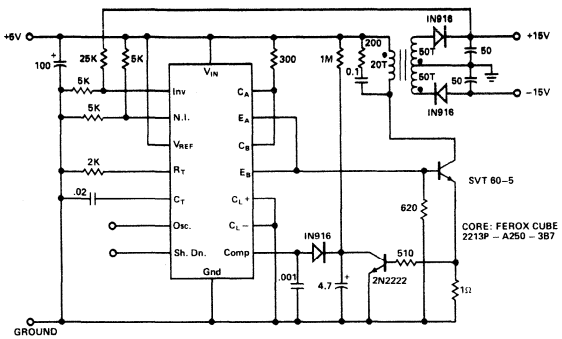


FIGURE 19 – +5 TO ±15 VOLT, FLYBACK CONVERTER

This circuit is designed to develop a regulated ±15 volt supply from a single +5 volt source. Note that the reference terminal is tied to the input, disabling the internal regulator. The error amplifier resistors are also tied to the input line so the output regulation can be no better than the input; however, an external reference could just as easily have been used.

In this application, the two output stages are connected in parallel and used as emitter followers to drive a single external transistor. Since the currents in the secondary of a flyback transformer are out of phase with the primary current, current limiting is very difficult to achieve. In this circuit, protection was provided through the use of a soft-start circuit. If either output is shorted, the transformer will saturate, providing more current through the drive transistor. This current is sensed and used to turn on the 2N2222 which resets the soft-start circuit and turns off the drive signal. If the short remains, the regulator will repetitively try to start up and reset with a time constant set by the soft-start circuit. Removing the short will then allow the regulating loop to re-establish control.

For higher current applications, the single-ended conventional switching regulator of Figure 20 is shown.

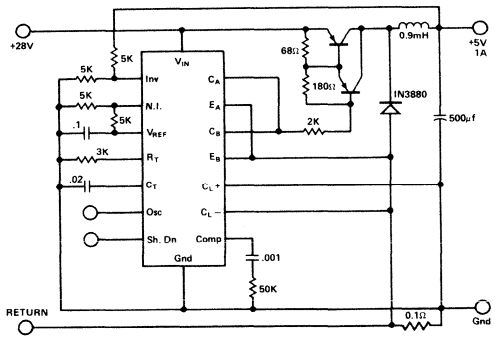


FIGURE 20 – 1 AMP, SINGLE-ENDED SWITCHING REGULATOR

In this case, an external PNP darlington is used to provide a 1-amp current switch. The SG1524 has the two outputs in parallel, connected as a grounded emitter amplifier. The current sense resistor is inserted in the ground line and the voltage across it used for constant current limiting. Note that in addition to the divider resistors and frequency setting $R_T C_T$, a phase compensation resistor and capacitor is used to stabilize the loop now that an inductor has been added.

A fourth application would have to be a push-pull, DC to DC regulating converter as shown in Figure 21.

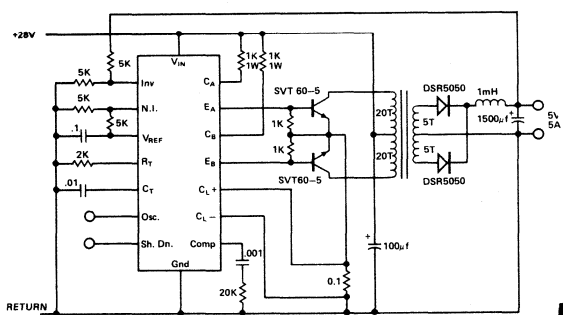


FIGURE 21 – 5V, 25W, DC TO DC CONVERTER

Here the outputs of the SG1524 are connected as separate emitter followers driving external transistors. Current limiting in this application is done in the primary for several reasons: First, it's easier to live within the ±1 volt common mode limits of the current limit amplifier; second, since this is a step-down application, the current – and therefore the power in the sense resistor – is lower; and third, if the output drive were to

become non-symmetrical causing the transformer to approach saturation, the resultant current spikes will shorten the pulse width on a pulse-by-pulse basis, providing a first order correction. Note that the oscillator is set to run at 40 kHz to obtain a 20 kHz signal at the transformer.

This application as shown does not provide input-output isolation and, of course, that feature is difficult to achieve within a single IC. There are a couple of ways the SG1524 can be used with isolated power supply systems, however. The first is shown in Figure 22 where the SG1524 is direct coupled

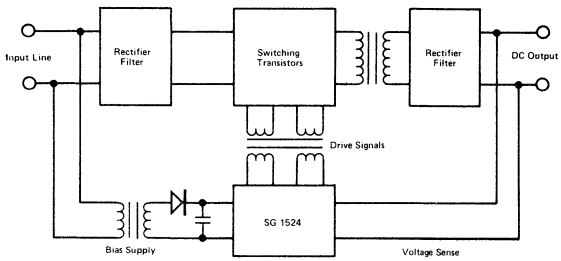


FIGURE 22 – INPUT/OUTPUT ISOLATION

on the secondary side of the output transformer. The outputs from the IC are transformer-coupled back to the primary side to drive the switching transistors. Of course, a separate start-up power source is needed for the SG1524 but that shouldn't present much of a problem remembering that the IC draws less than 10 mA of supply current.

A different method of providing isolation is shown in Figure 23 where the IC is direct coupled on the primary side. Here a separate reference and error amplifier (most easily implemented with a SG723 regulator IC) is connected on the secondary and then optically coupled back to the primary side.

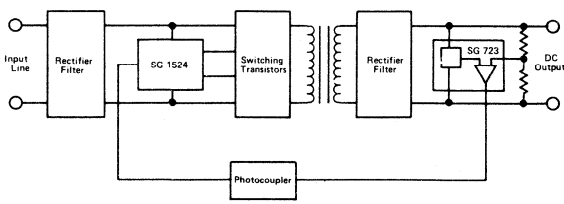


FIGURE 23 – INPUT/OUTPUT ISOLATION

As should be evident from the above, the SG1524 was designed as the first of what will undoubtedly become a larger family of regulator ICs specifically designed for switching power supplies. As such, versatility was the primary design goal of this device and hopefully this goal has been achieved to the degree that will allow the SG1524 to find application to a wide range of power control systems.

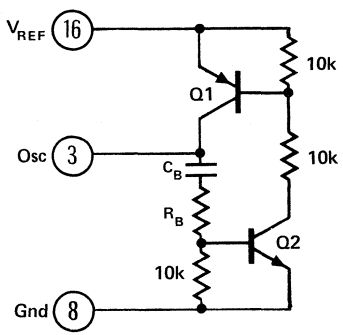
DEADBAND CONTROL WITH THE SG1524 REGULATING PULSE WIDTH MODULATOR CIRCUIT

The SG1524 Regulating P.W.M. integrated circuit provides two outputs which alternate in turning on for push-pull inverter applications. The internal oscillator sends a momentary blanking pulse to both outputs at the end of each period to provide a deadband so that there cannot be a condition when both outputs are on at the same time. The amount of deadband is determined by the width of the blanking pulse appearing on pin 3 and can be controlled by four techniques:

1. For 0.2 to 1.0 microseconds, the deadband is controlled by the timing capacitor, C_T, on pin 7. The relationship between C_T and deadband is shown in Figure 3 on the SG1524 data sheet. Of course, since C_T also helps determine the operating frequency, the range of control is somewhat limited.

2. For 0.5 to 3.0 microseconds, the blanking pulse may be extended by adding a small capacitor from pin 3 to ground. The value of the capacitor must be less than 1000 pf or triggering will become unreliable.

3. For longer and more well-controlled blanking pulses, a simple one-shot latch similar to the circuit shown below should be used:



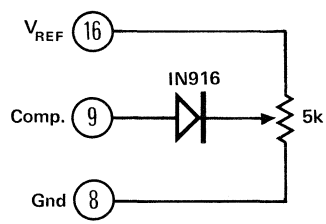
TRANSISTORS — Small-signal general purpose types.
For 5 μsec width, C_B = 200 pf, R_B = 10k

When this circuit is triggered by the oscillator output pulse, it will latch for a period determined by $C_B R_B$ providing a well-defined deadband.

Another use for this circuit is as a buffer when several other circuits are to be synchronized to one master oscillator. This one-shot latch will provide an adequate signal to insure that all the slave circuits are completely reset before allowing the next timing period to begin.

Note that with this circuit, the blanking pulse holds off the oscillator so its width must be subtracted from the overall period when selecting R_T and C_T.

4. Another way of providing greater deadband is just to limit the maximum pulse width. This can be done by using a clamp to limit the output voltage from the error amplifier. A simple way of achieving this clamp is with the circuit below:



This circuit will limit the error amplifier's voltage range since its current source output will only supply 200μA. Additionally, this circuit will not affect the operating frequency.

IMPROVING SWITCHING REGULATOR DYNAMIC RESPONSE

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ABSTRACT

Recent introductions of LSI integrated circuits for P.W.M. control have offered considerable simplification to the job of optimizing the design of switching regulators. In addition to greatly reducing the necessary circuitry, the linear transfer function of these devices eases the task of stabilizing the feedback loop and offers several possibilities for improved response. Experimental methods for evaluating the response characteristics of the P.W.M. switching and output stages can be used to confirm simplifying assumptions of linear operation. With this data, several approaches to equalization networks can be compared for performance optimization.

The past few years have seen a major revolution take place in the field of power supply design. Whether forced upon us by the need for energy conservation or finally made practical thru recent advances in semiconductor technology, switching regulators are now the name of the game in voltage control. Novices soon learn, however, that the implementation of a well-designed switching supply involves a little more skill than that required for a linear regulator.

Although the theory of switching regulation has long been known, there is much practical technology – or art – in designing efficient and reliable systems. This is still true even though recently introduced semiconductor devices have made the job at least a little easier. It is the purpose of this discussion to cover a few of the practical aspects of implementing and stabilizing switching regulators using these newer devices.

6

INTEGRATED P.W.M. CONTROL CIRCUITS

Recognizing a rapidly growing market, many component suppliers have introduced new devices designed specifically for switching regulator applications. These include faster power transistors with improved S.O.A., low E.S.R. electrolytic capacitors, hybrid power devices which include a matched commutating diode,[1] and monolithic IC control devices such as the SG1524[2] which contain all of the P.W.M. control circuitry in a single 16-pin, dual-in-line package.

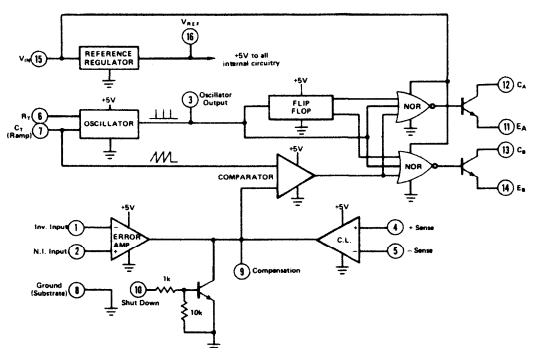


Figure 1. SG1524 Block Diagram

From the block diagram shown in Figure 1, it can be seen that the SG1524 contains the elements necessary to implement either single-ended switching regulators or DC to DC converters of several different configurations. This device includes a voltage reference, error amplifier, constant frequency oscillator, pulse width modulator, pulse steering logic, dual alternating output switches, and current limiting and shutdown circuitry. Since many of the different types of applications for this IC have been discussed earlier[2] it should suffice to review only two of the more common usages as shown in Figures 2 and 3.

The single-ended regulator of Figure 2 is unique because of its simplicity. This circuit combines an SG1524 with a Unitrode PIC-625 to build a 5 volt, 5 amp regulator with all the semi-

conductor devices contained in only two packages. This circuit has an efficiency of over 70% with an input voltage range of 20 to 30 volts, 0.1% line and load regulation, and some added benefits of constant frequency operation and short circuit protection.

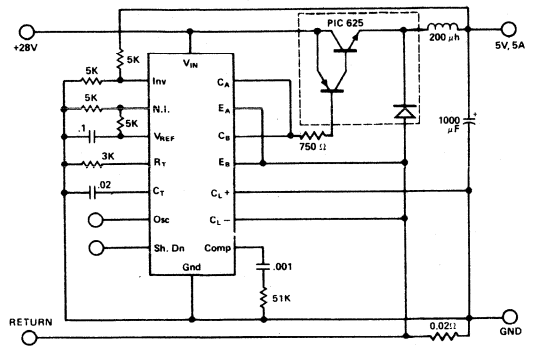


Figure 2. SG1524 Single-Ended Switching Regulator

Figure 3 shows the same 5-volt, 5 amp output requirement met this time with a DC to DC converter. The use of high speed transistors and Shottky rectifiers keep the efficiency more than 80% – significant for a low-voltage output – while maintaining all the other benefits included in the single-ended circuit.

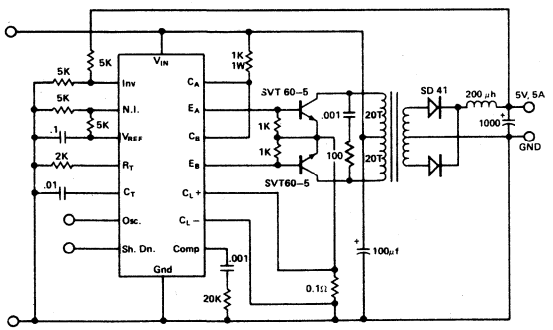


Figure 3. SG1524 Regulating DC-DC Converter

It should be recognized that the above circuits represent very basic applications of an IC control chip. Most practical power supply systems would probably incorporate many other features which may be accomplished by interfacing these IC's with a small amount of external circuitry to add characteristics such as: soft-start, oscillator synchronization, dead-band controls, additional current and/or voltage step-up stages, input-output isolation, remote overvoltage or overload shutdown, and response modifying circuitry. It is this latter subject we wish to explore more fully below.

SWITCHING REGULATOR CONTROL

The basic switching regulator control loop which applies to the most common forms of implementation is illustrated in Figure 4. In analyzing this control loop stability, the obvious immediate problem is the transfer function of the P.W.M. and output stage. A detailed and accurate analysis of the nonlinear characteristics of this stage is an extremely difficult and complex task if one is to account for all the parameters which could possibly be a factor.[3,4,5] On the other hand, if this stage could be assumed to have a linear transfer function, analysis becomes a relatively simple application of basic feedback theory.

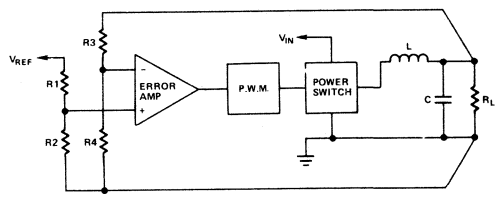


Figure 4. Basic Regulating Control Loop

A significance of the SG1524 is that it uses a design approach which makes a linear assumption accurate enough for most applications. The fact that this device features constant frequency operation, a linear-slope ramp for P.W.M., and fast-response logic and output circuitry all contribute to minimizing the errors associated with a linear assumption. Of course, there are factors external to the IC which could destroy this assumption. Such things as excessive delay in the switching transistors, parasitic ringing or oscillation in the power stages, or nonlinear operation of the magnetics could all cause a resultant nonlinear performance. A first exercise for the designer, then, is to confirm linear operation of the P.W.M. and output stages of his regulator by evaluating his early breadboard models.

OUTPUT STAGE ANALYSIS

The pulse width modulation is accomplished in the SG1524 by comparing the output of the error amplifier with a linear ramp, or saw-tooth signal from the oscillator. Because the comparator has both high gain and high input impedance, and the error amplifier has a high output impedance, this node (pin-9) becomes a very convenient place for inserting a test signal. A voltage source applied as shown in Figure 5 will completely override the error amplifier and essentially open the loop without actually breaking any connections. In addition, the test signal is easily managed because the voltage gain from this point

to the output is relatively low. (A voltage level on pin 9 of from 1 to 4 volts will change the pulse width from zero to maximum which will yield zero to maximum output voltage.)

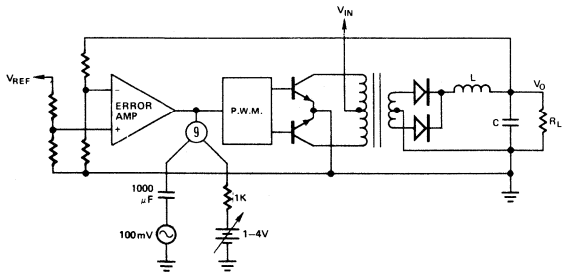


Figure 5. Measuring Output Stage Transfer Function

In experimentally attempting to confirm satisfactory operation of the output stages, the designer hopes to prove that a linear equivalent circuit model is valid for reasonable analysis. One such model as proposed by Middlebrook[6] is shown in Figure 6. This model describes the overall AC and DC transfer function and input and output impedances in terms of the duty cycle and modulation constant. This model assumes that the effects of operating frequency, switching delays, and parasitic elements are well above the frequencies of interest as defined by the output LC filter.

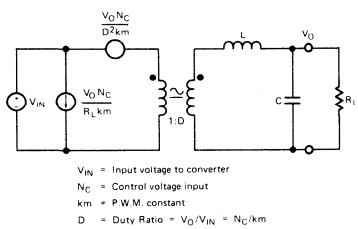


Figure 6. Linear Equivalent Circuit

Values for the inductor and capacitor are normally calculated on the basis of output ripple current and voltage as follows:

For constant frequency operation,

$$L = \frac{V_O(V_{IN} - V_O)}{V_{IN} f(\Delta I_L)}$$

and

$$C = \frac{V_O(V_{IN} - V_O)}{8Lf^2 V_{IN}(\Delta V_O)}$$

where:

V_{IN} = peak input voltage to the inductor
V_O = output voltage across the capacitor
f = switching frequency
ΔI_L = peak-to-peak current variation in the inductor
ΔV_O = peak-to-peak ripple voltage across the capacitor.

Note that the actual ripple voltage at the output of the filter will be ΔV_O, plus ΔI_L times the capacitor E.S.R.

Regardless of the requirements for minimizing the output ripple, an additional requirement on the filter is that its cutoff frequency be well below the switching frequency if our original goal of simple linear analysis is to be met. Specifically, the switching operation introduces a second order lag at one-half the switching frequency and for the output filter to dominate, its cutoff should be at least an order of magnitude below that number, or

$$\frac{1}{2\pi\sqrt{LC}} \leqslant \frac{f}{20}$$

To verify the performance of the resultant hardware, a Bode plot of the output stage response can be most meaningful. Ideally, a plot as shown in Figure 7 should show a flat response to the filter cutoff and then a linear 12 dB/octave rolloff with a

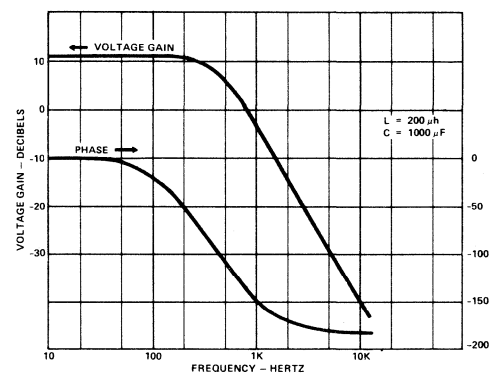


Figure 7. Linear Output Stage Response

180° phase shift. By making these plots with varying input voltage and load current, factors affecting stability such as leakage inductance, capacitor E.S.R., and either saturation or discontinuous operation of the magnetics may be evaluated over the operating conditions of interest. Figure 8 shows typical plots with less than ideal component parameters. With the characteristics of the output stage defined, attention can be turned to the error amplifier to develop an equalizing network which will allow satisfactory closing of the loop.

ERROR AMPLIFIER COMPENSATION

The error amplifier contained within the SG1524 is a transconductance amplifier in that it has a high-impedance, current source output. The gain is a function of the output loading and

can be reduced from a nominal 80 dB by shunt resistance as shown in Figure 9. Note also in Figure 9 that the uncompensated amplifier has a single pole at 300 Hz and 90° of phase shift. The unity gain cross-over frequency is 3 MHz and the large scale slew rate is 0.5 volt per microsecond.

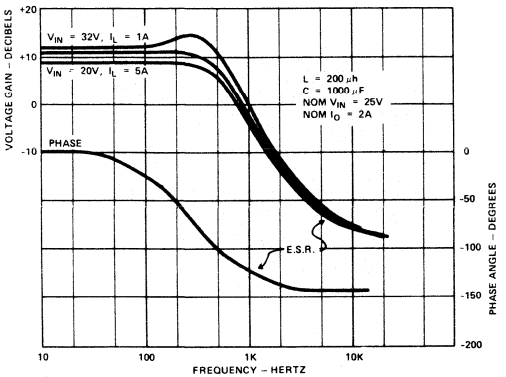


Figure 8. Measured Output Stage Response

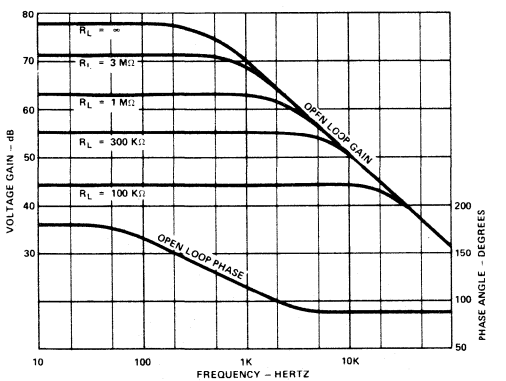


Figure 9. Open-Loop Error Amplifier Response

This type of amplifier can be compensated in two ways: The compensation network can go from the output to ground or it can be connected from output back to the inverting input.(7) In the first case, the voltage gain is:

$$A_V = gmZ_C = \frac{8I_CZ_C}{2kT} \approx 0.002Z_C$$

where Z_C is the complex compensation network impedance. If a feedback approach is used, the gain is:

$$A_V = \frac{Z_C}{Z_S}$$

where Z_S is the source impedance driving the input. In cases where relatively low impedances are desired in a feedback network, it may be necessary to buffer the high output impedance of the error amplifier. Figure 10c shows the use of an external emitter follower to provide a low driving impedance for the feedback network.

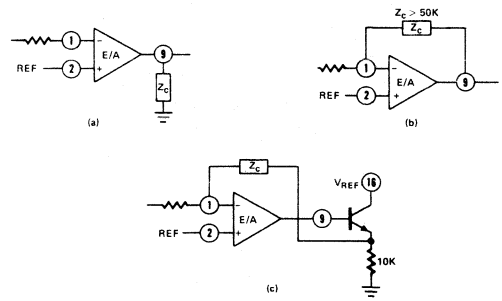


Figure 10. Error Amplifier Compensation Networks

To stabilize the overall regulator feedback loop of Figure 4, it should be apparent that the uncompensated loop contains at least two poles in the output filter and one more in the error amplifier, a situation which typically results in significant gain remaining when the total loop phase equals 360°. One of the simplest compensation schemes is to convert the error amplifier to an integrator by adding a single dominate pole at a frequency so low that the loop gain falls below unity well before the cut-off frequency of the output filter. While this approach yields a stable closed loop gain as shown in Figure 11, the response to disturbances is very slow. For example, the waveforms of Figure 12 show the response to a 20%, or one amp, step change in load to the circuit of Figure 3 when compensated with a 0.2 mfd capacitor around the error amplifier.

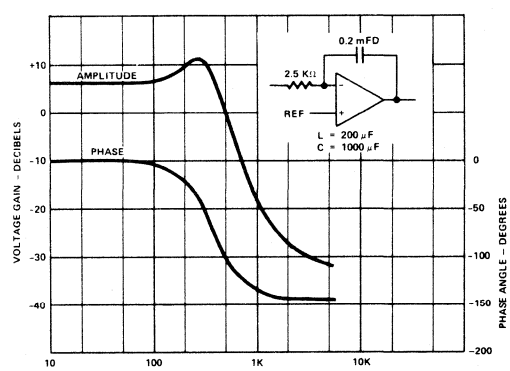
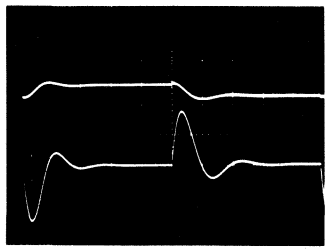


Figure 11. Closed Loop Frequency Response

If instead of slowing down the error amplifier, a zero, or lead network is added to cancel one of the output filter poles, we can keep the total loop phase less than 360° to well beyond the output filter cutoff.



STIMULUS: ONE AMP STEP CHANGE IN I_O
UPPER TRACE: ERROR AMP OUTPUT, 500 mV/DIV
LOWER TRACE: REGULATOR OUTPUT, 200 mV/DIV
TIME BASE: 5 MILLISECONDS/DIV

Figure 12. Integrator Compensation Step Response

Figure 13 shows a circuit for accomplishing this by moving the amplifier pole lower in frequency and adding a zero at the output filter cutoff frequency. Figure 14 shows the effects of this network on the Bode plot of the error amplifier, and Figure 15 indicates the improvement in recovery from the same one-amp load change. Note how the output of the error amplifier overshoots to give a boost to the output.

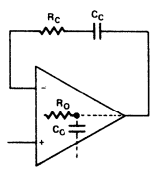


Figure 13. Series RC Phase Compensation

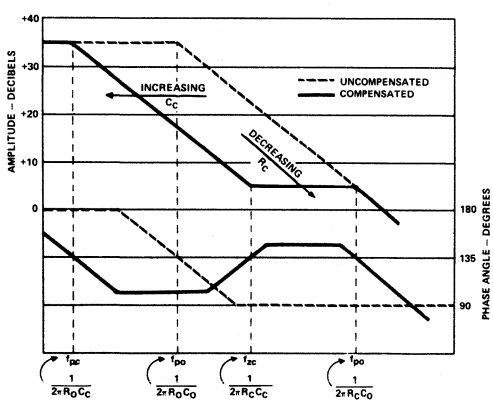
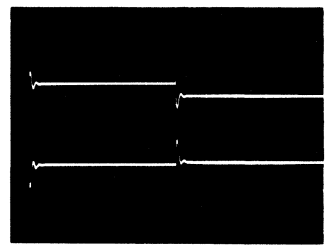


Figure 14. Phase Compensated Bode Plot

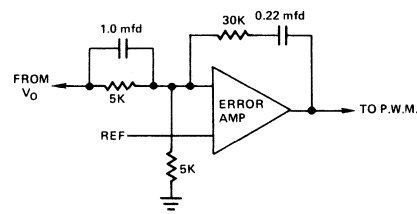
Even faster response can be achieved by providing additional lead networks. For example, another zero may be added by bypassing the sense feedback resistor. As can be seen in Figure 16, this greatly improves loop response but offers the hazard of coupling ripple noise directly into the error amplifier.

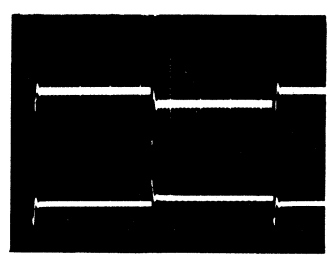


R_C = 30 KΩ, C_C = .022 mfd

STIMULUS: ONE AMP STEP CHANGE IN I_O
UPPER TRACE: ERROR AMP OUTPUT, 500 mV/DIV
LOWER TRACE: REGULATOR OUTPUT, 100 mV/DIV
TIME BASE: 5 MILLISECONDS/DIV

Figure 15. Phase Compensated Step Response





STIMULUS: ONE AMP STEP CHANGE IN I_O
UPPER TRACE: ERROR AMP OUTPUT, 500 mV/DIV
LOWER TRACE: REGULATOR OUTPUT, 50 mV/DIV
TIME BASE: 2 MILLISECONDS/DIV

Figure 16. Double Zero Compensated Step Response

TWO LOOP CONTROL

From the examples presented above, it should be apparent that the integration method of error amplifier compensation provides good stability by making the dominate pole so low in frequency that variations in all other circuit parameters become inconsequential. This technique also provides high accuracy at DC where high gain can be used and is the type of feedback one would want to take directly from the output of a regulator since a user might add additional external capacitance, thereby

changing the output filter characteristics. Another reason for using single-pole compensation is to accommodate the use of a two-stage output filter which can add phase shifts well beyond 180°.

The problem of poor response can then be accommodated by adding a differentiated signal taken from somewhere else in the loop. If the time constants and gain factors are properly selected, the differentiated signal can compensate for the error in the integrated signal taken from the regulated output.

While it may be possible to combine these two signals with passive signal conditioning at the input to the error amplifier, a more straightforward approach is with two separate op amps as shown in Figure 17. Here the error amplifier in the SG1524 has

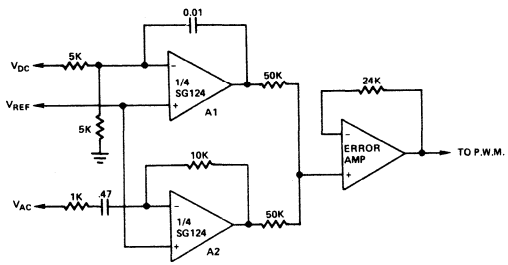
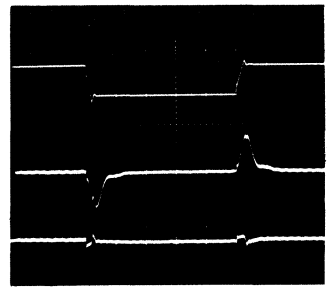


Figure 17. Two-Loop Signal Conditioning

been connected as a unity gain summing amplifier and two op amps from an SG124 quad IC are used as gain stages for signal conditioning. Since these are single-supply op amps, they are powered directly from the 5-volt reference voltage supplied by the SG1524.

Amplifier A1 provides the DC gain and gets its signal directly from the output of the regulator. There are several possibilities, however, for providing the differentiated correction signal through A2. If rapid response to changes in input voltage is required, A2's input may be taken through a resistive divider directly to the input line.[8] This is, of course, not a feedback signal but the feed forward of an open loop, short-duration correction signal. The waveforms of Figure 18 show the improvement which this feed-forward signal can offer.

If load transients are the problem, A2's input might be connected to a point where output current could be sensed. This would best be accomplished by using a current transformer in series with the output capacitor although the voltage across the capacitor E.S.R. might also serve as a sense point. In either case, a low-pass filter with a cuttoff frequency of approximately 1/4



UPPER TRACE: INPUT VOLTAGE STEP CHANGE, 5V/DIV
MIDDLE TRACE: OUTPUT WITH DC FEEDBACK ONLY, 100 mV/DIV
LOWER TRACE: OUTPUT WITH AC FEED FORWARD ALSO, 100 mV/DIV
TIME BASE: 2 MILLISECONDS/DIV

Figure 18. Feed Forward Compensation

the switching frequency is necessary to remove the ripple voltage before attempting a differentiation. A third possible signal input is to put a secondary winding on the output filter inductor. This gives an AC signal proportional to $V_{IN} - V_O$ and will therefore respond to disturbances at either input or output.

SUMMARY

Although integrated circuit controllers for switching supplies have removed much of the circuit complexity from this type of regulator, the dynamic analysis of the control loop must still be optimized for each application. This optimization is made easier, however, if a linear approximation of the switching stages can be shown to be valid. The SG1524 controller offers benefits in this regard as it does provide a linear transfer function through its pulse width modulation scheme. Therefore, experimental techniques can be used to simply confirm proper operation of the power switches and output filter.

With a linear output stage, conventional feedback analysis can be used to define the best equalizing network achieving a compromise between stability and fast response. In some cases it may even be desirable to provide separate signal paths for these two parameters but thus, too, can be adapted to the SG1524 controller with a minimum of external circuitry.

Obviously, no recipes for optimum performance have been provided herein. Only a few directions which, it is hoped, will point the way toward the development of specific solutions for specific applications.

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THE OUTPUT SUPERVISORY CIRCUIT
A NEW ANALOG LSI CIRCUIT FOR POWER SUPPLY CONTROL

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ABSTRACT

This paper describes a new monolithic integrated circuit which contains all the functions necessary to monitor and control the output of a sophisticated power supply system. Sensing for over and under-voltage conditions, current sensing and an SCR crowbar firing circuit are all contained on this single IC along with an independent, accurate reference generator. A description of the operation of each individual circuit is given along with several applications which demonstrate the utility of the device.

Introduction

Recent years have seen the introduction of many sophisticated integrated circuits for use in controlling the voltage regulation function of both linear and switching power supply systems. While these circuits have provided a high degree of performance with a side benefit of considerable increases in both reliability and cost savings, they have all addressed the basic function of maintaining the output voltage constant. Most power supply systems, however, require additional circuitry for monitoring satisfactory performance and providing protection in the event of a fault condition. These requirements have led to the development of a new class of power supply element — an Output Supervisory Control Circuit.

The SG1543 Output Supervisory Circuit

To fill the need for this output monitoring and controlling function, the SG1543 output supervisory circuit shown in Figure 1 was developed. This device contains an operational amplifier, a voltage reference circuit, several comparators, and a high-current SCR trigger circuit. The functions performed by this device include over-voltage and under-voltage sensing, current limiting, and provisions for triggering an external SCR crowbar shutdown. All the functions provide open collector outputs for maximum flexibility in interfacing with either the power supply or the system load and, although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs or by an external shutdown command. The SCR trigger circuit also includes an optional latch with external reset capability. External capacitors may be used to accurately program the sensing circuits for a minimum time duration of fault before triggering.

The SG1543 circuit may be powered by either the output voltage to be monitored or a separate bias voltage at any level between 4.5 and 40 volts with a standby current of less that 10mA.

SG1543 BLOCK DIAGRAM

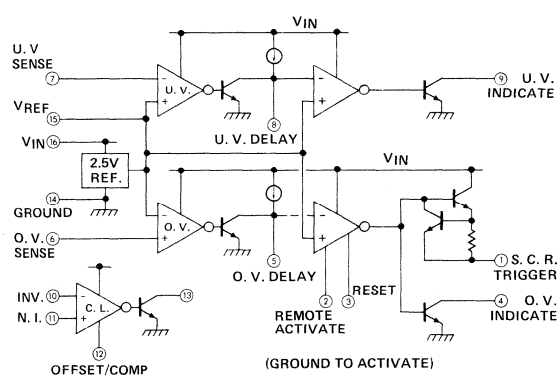

Figure 1. The block diagram of the SG1543 Output Supervisory Circuit includes over-voltage and under-voltage sensing as well as the capability for current limiting and SCR crowbar triggering.

This device is packaged in a standard 16-pin hermetically sealed ceramic package and is available in both commercial and military temperature ranges. Before describing in greater detail the overall functions that this device can perform, it is worth discussing the individual circuits which go into its makeup.

Voltage Reference Circuit

The precision 2.50V reference circuit of the SG1543 is shown in Figure 2. This regulator is based upon the well-known band gap reference circuit which has the capability of providing very stable performance over an input voltage range from as low as 4.5V to as high as 40V. The output is nominally set at 2.50V, but in addition, is trimmed to remove all effects of production manufacturing tolerances from the output voltage. In fact, this trimming not only adjusts the output voltage to within 1% of 2.50V, but in the process, as shown in Figure 3, also trims the temperature coefficient of output voltage to better than 50 parts per million per degree C. The trimming is performed at wafer probe by using controlled energy sources to blow fusable metal links which short out incremental values of resistance in the voltage setting network. These resistors are binarily coded so that three values give eight bits of resolution and allow trimming to better than ±12 millivolts. With this accuracy, in all but the most precise applications, the need for adjustment or trimming potentiometers is effectively eliminated.

The output of this reference circuit is current limited for protection and will provide up to 10 milliamps of current for use as a reference for other functions that may be required along with the SG1543. In addition to stable temperature performance, this regulator also maintains its output voltage to within 10mV for all line and load changes. Additional benefits of the band gap reference circuit include low noise performance, instant turn-on, and a high degree of long-term stability.

PRECISION 2.50 VOLT REFERENCE

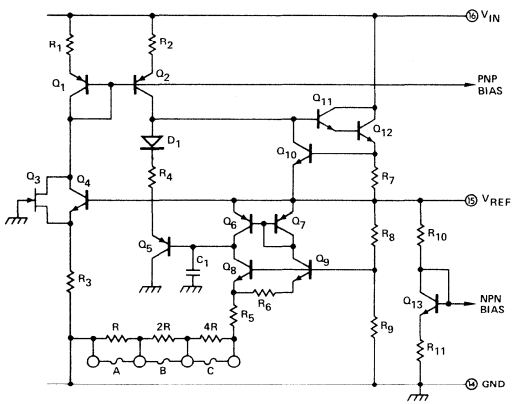

Figure 2. This precision 2.50 volt band-gap reference source is internally trimmed for ±1% accuracy in order to eliminate the need for adjustment potentiometers.

CHANGE IN TEMPERATURE COEFFICIENT WITH REFERENCE VOLTAGE TRIM

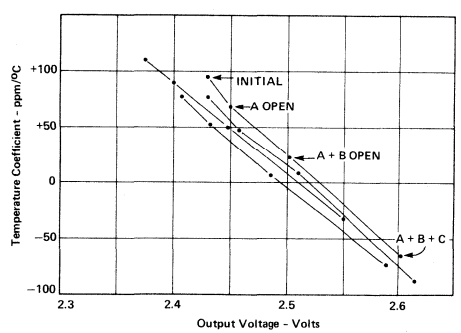

Figure 3. As successive links are opened in the reference voltage trimming network, the output voltage increases and the temperature coefficient becomes less positive.

Comparator Section

Over and under-voltage sensing circuits are identical with only the input polarity changed between them. The under-voltage circuit is shown schematically in Figure 4. This configuration is made up of two comparators in series, each referenced to 2.50 volts, with the delay terminal at their juncture. The first comparator activates a current source upon sensing an out of tolerance condition and that current is used to charge an externally selected capacitor to provide a delay. The second comparator then activates the output indicating circuit. The overall time delay from

VOLTAGE SENSING COMPARATORS

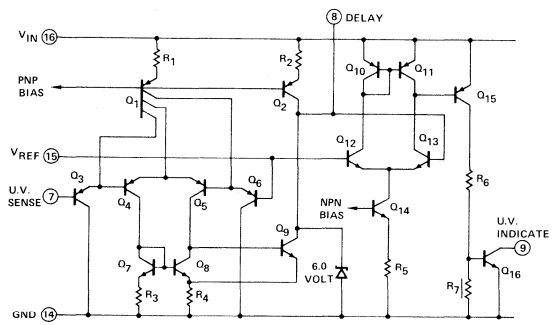

Figure 4. Voltage level sensing is done with a high input impedance comparator with built-in hystersis. When switched, the input comparator allows a constant current source to trigger the output comparator.

input sense to output indicate, with no external capacitor, is approximately 0.5 microsecond. By adding a capacitor at the delay terminal, the fault must exist for an interval defined by the time it takes the voltage on the capacitor to charge from zero to 2.5V before the output comparator can switch. The charging current for this capacitor is a constant 250 microamps which provides for a delay of approximately 10 milliseconds per microfarad of capacitance. Since the comparator can discharge in excess of 10mA, the capacitor is reset in a fraction of its charge time.

The input comparator has PNP transistor inputs which provide both high input impedance with less than one microamp bias current, and a wide input voltage range which includes ground and goes to within 2V of the positive supply voltage. Because the input PNP operates as an emitter follower, the input impedance to that comparator remains high throughout the input range. To eliminate the tendency to oscillate at threshold, a hysterisis of approximately 25mV is built into the input comparator.

The output indicating transistor, Q18, is designed to sink 10mA of current with a saturation voltage of less than 0.4 volt. Its open collector allows several outputs to be connected together to provide a single indicating signal.

SCR Trigger Section

While the under-voltage sensing circuit has only the 10mA, or low current, open-collector output, the over-voltage section contains additionally, an SCR crowbar triggering circuit good for 250mA. This stage also includes provisions for remote activation of the output as well as a reset terminal. From the schematic shown in Figure 5, it can be seen that the ouput voltage comparator drives a PNP transistor, Q6, with two collectors, one of which drives the low-current, open collector indicating signal similar to the under-voltage circuit. The other collector of Q6 drives a darlington amplifier which will provide 250mA to activate an external high current SCR crowbar device. Note that these two outputs are complements of each other; i.e. when pin 4 switches to ground, pin 1 goes positive.

OVER-VOLTAGE CIRCUIT

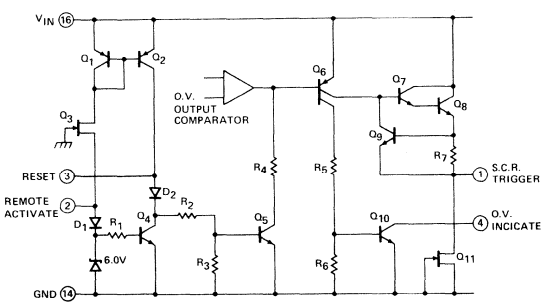

Figure 5. Either the over-voltage output comparator or the remote activation terminal will energize both the SCR trigger and the O.V. indicating transistor. Connecting pins 4 and 2 form a latch.

Since in many cases it is desired to activate the crowbar under other than over-voltage conditions, a remote activation circuit is also included. This consists of transistors Q1 through Q5 as shown in Figure 5. The functioning of this circuit is as follows: Q3 provides a controlled current source of approximately 300 microamps to saturate transistor Q4. With Q4 saturated, transistor Q5 is held in the off condition. When the remote activation terminal, pin 2, is grounded, it diverts the current away from the input of Q4, turning it off and turning Q5 on, which activates the output circuitry in the same manner as the over-voltage comparator.

An additional function of this circuit is to provide the capability to latch the outputs on after a fault is sensed, by externally connecting the over-voltage indicating terminal, pin 4, to the remote activation terminal, pin 2. With this configuration, an over-voltage condition which turns on Q10 will pull pin 2 to ground activating the remote activation signal which, in turn, holds the circuit in the on condition until the reset terminal is externally grounded, removing the latch and turning off the output. Thus, the user has the capability to either activate the high current output only as long as a fault condition exists, or to latch it on upon the occurrence of a fault requiring external action by an operator to reset the circuit to its initial condition. Thresholds for both remote activation and reset terminals are approximately 1.2 volts.

Current Sensing Amplifier

The amplifier in the SG1543 designated for current sensing actually has much wider application. It is basically a high-gain, non-compensated operational amplifier with an open collector output; i.e., pull-up on the output must be provided externally. From the schematic shown in Figure 6, it can be seen that this circuit also has a PNP front end which gives it a wide common-mode range extending from slightly below ground to within 2 volts of the supply voltage. With a pull-up resistor of 2kΩ, the open loop voltage gain is greater than 72dB with a unity gain bandwidth beyond 5MHz. When used as a comparator, the response time is less than 200 nanoseconds, and if linear amplification is required, external compensation may be added for stable performance over a wide frequency range or a unique frequency response.

The input to this amplifier is balanced for zero offset voltage but a fixed offset or threshold of up to 200mV may be incorporated by adding or subtracting current

CURRENT–SENSING AMPLIFIER

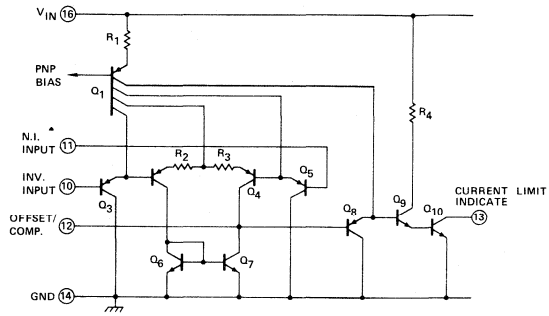

Figure 6. PNP inputs give the current limit amplifier a common-mode input voltage range of from below ground to within 2 volts of the supply voltage.

C.L. AMPLIFIER FREQUENCY RESPONSE

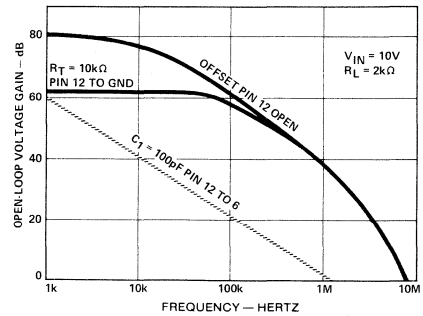

Figure 8. With 80dB gain and 5MHz bandwidth, the current sense amplifier provides a wide dynamic response, even when modified with external passive components.

at the offset/compensation pin 12. For most current sensing applications the required threshold polarity calls for a positive voltage on the inverting input. This can be accomplished with a resistor, R_T, to ground as shown in Figure 7.

Reducing the impedance at pin 12 also lowers the gain of the amplifier somewhat as shown in Figure 8. This fact allows pin 12 to do double-duty as a point to apply frequency compensation as well. Due to the excess phase shift of the internal PNP transistors, this amplifier requires compensation for stable closed-loop, linear applications but this can be accomplished easily with either C1 to the output or C2 to ground as shown in Figures 7 and 8.

Diode D1 and resistor R_C are used only if it is necessary to increase the frequency response by operating the output transistor at higher current and/or isolating the load from R_C and C1 when the amplifier is off.

CURRENT SENSE COMPENSATION

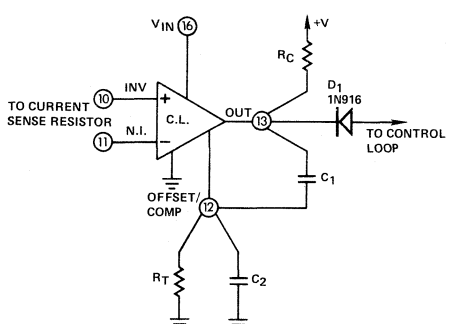

Figure 7. External components can be used with the current sense amplifier to establish an input offset or threshold, define the frequency response, and buffer the output.

Applications

Figure 9 shows a typical application of the SG1543 as used to monitor a single power supply output voltage for both high and low voltage operation as well as current limiting. The data accompanying Figure 9 indicates how the values for the external components are selected. This circuit is driven from an external bias supply which must provide a standby current of 10mA maximum plus the activation current for the SCR trigger. The application in Figure 9 shows a single resistor divider string, R4, R5 and R6, which sets the thresholds for both the under and over-voltage activation levels. The external capacitors CD1 and CD2 are used to provide time delays before activation of the output circuitry. The output of the comparators can be used for many different functions; in this case, they are shown driving indicators. They can also provide signals to the system under power to give information that an out-of-tolerance condition exists. Additionally, by the external connection between pin 2 and pin 4, a latch has been provided such that an over-voltage condition will activate and hold that control signal until positive reset action at pin 3 is performed.

In firing an SCR with supply voltages above 5 volts an external resistor, RG, is used on pin 1 to provide power dissipation limiting for the SG1543. While the SG1543 will provide up to 250mA of trigger current, the power limitation of the 16-pin dual-in-line package should be held to less than one watt.

In this application, current limiting is performed by sensing the current in the positive supply line with fold-back provided by the action of R2 and R3. A fixed threshold for the amplifier is set by R1 which is connected between pin 12 and ground.

Although the SG1543 could have been driven from the output voltage to be monitored, it would lose control when that output voltage fell to approximately 3V. This

would, of course, preclude the use of the current limit function where short circuit protection must be provided.

SG1543 TYPICAL APPLICATION

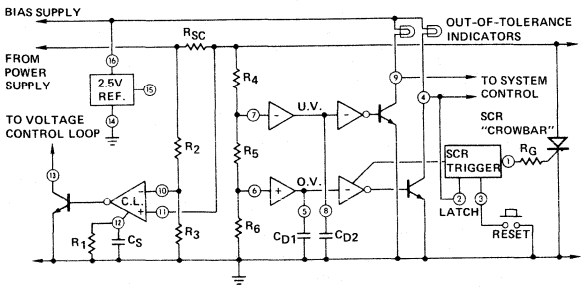

Figure 9. This typical application for the SG1543 provides linear foldback current limiting as well as over and under-voltage protection.

The values for the external components used in conjunction with the SG1543 application of Figure 9 are determined as follows:

Current limit input threshold, $Vth \approx \frac{1000}{R1}$

Cs is determined by the current loop dynamics

Peak current to load, $Ip \cong \frac{Vth}{Rsc} + \frac{Vo}{Rsc}\left(\frac{R2}{R2 + R3}\right)$

Short circuit current, $Isc = \frac{Vth}{Rsc}$

Low output voltage limit, $Vo\ (Low) = \frac{2.5\ (R4 + R5 + R6)}{R5 + R6}$

High output voltage limit, $Vo\ (High) = \frac{2.5\ (R4 + R5 + R6)}{R6}$

Voltage sensing delay, $td = 10{,}000\ Cd$

SCR trigger power limiting resistor, $Rg > \frac{Vin - 5}{0.2}$

Current Sensing Options

It is important to remember that all the features of the SG1543 apply equally to either linear or switching power supplies. Figure 10, for example, shows the current sensing amplifier in the SG1543 used to provide foldback current limiting for a linear regulator utilizing the SG723. To answer the question of why one would use the SG1543 for current limiting when that capability is built into the SG723, there are two important benefits: low sensing threshold voltage (whatever is selected vs. a fixed 700mV) and much higher gain for a very sharp transition from voltage to current feedback.

Output current limiting for a switching supply which gets its control from an SG1524 regulating pulse width modulator is shown in Figure 11. Here, foldback is not included but an optical coupler for isolation has been added. It should be noted that all the low-current outputs of the SG1543 are equally well suited for driving optical couplers.

LINEAR FOLDBACK CURRENT LIMITING

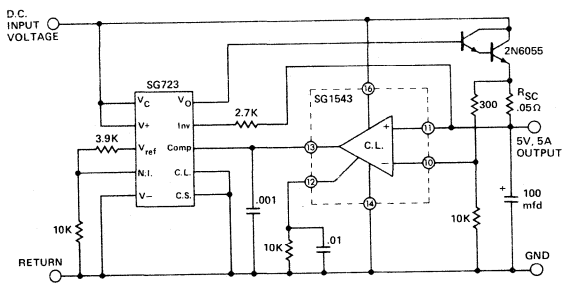

Figure 10. The SG1543 is equally adaptable to either linear or switching supplies. The circuit above shows a substantially improved current limit function for a linear SG723 voltage regulator.

DC CONVERTER WITH ISOLATED CURRENT LIMITING

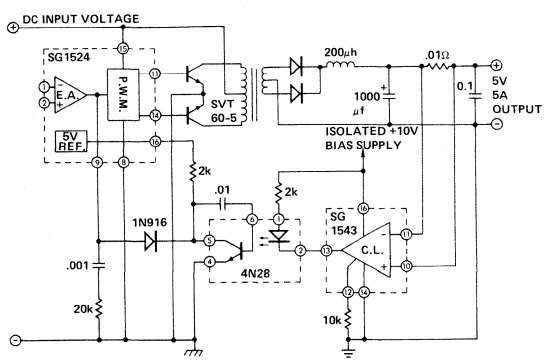

Figure 11. Current limiting for a switching inverter is readily accomplished, even with a requirement for input-output isolation.

This last application suggests another use for the current sense amplifier completely disassociated with current. This is shown in Figure 12 where it is used in conjunction with the very excellent characteristic of the 2.50 volt reference contained within the SG1543 to

provide an isolated voltage feedback signal. The SG1543's amplifier provides the gain and the overall loop compensation network, and drives a high-frequency opto-coupler which feeds into the unity-gain configured error amplifier of the SG1524. A designer should recognize that there are many possible variations on this theme, including taking the error signal from the collector of the opto-coupler, feeding it into the output of the SG1524's error amplifier such that this amplifier provides a startup signal. Then the SG1543 may be powered directly from the output eliminating the need for an isolated bias supply.

USING THE CURRENT SENSE AMPLIFIER FOR ISOLATED VOLTAGE FEEDBACK

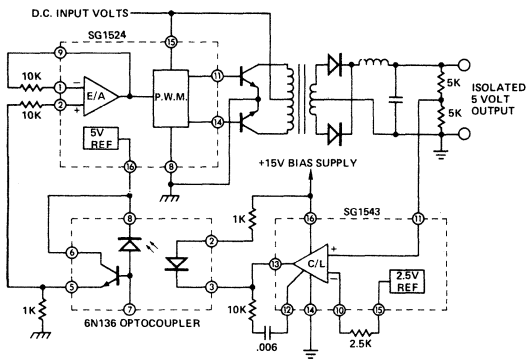

Figure 12. The current sense amplifier can also be used in conjunction with the SG1543's reference to provide a stable, isolated voltage feedback signal.

One final possible use for the current limit amplifier is to provide complete shutdown of the power supply rather than linear voltage reduction upon sensing an over-current condition. This function is shown in Figure 13 where the current limit amplifier is used as a comparator with the output terminal connected to the remote activation terminal for the SCR trigger. In this case, sensing is done in the ground line. There is no offset added to the current limit amplifier but instead a threshold is provided by the action of R1 and R2 from the 2.50V reference signal. When an over-current condition is sensed and maintained for a period of time determined by a capacitor CD on pin 12, then the ouput transistor will conduct, activating the SCR trigger and shutting down the power supply.

OVERCURRENT SHUTDOWN

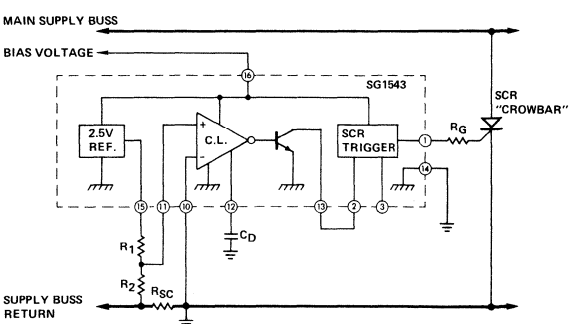

Figure 13. The current sense amplifier may also be used as a high-gain comparator to shut down the supply upon over-current.

Sensing Multiple Output Voltages

Most sophisticated power supply systems have several output voltages which need to be monitored, and this can also be accommodated easily with the SG1543 because of the capability for remote activation and the availability of the reference voltage for use with external circuitry. A simple quad comparator like the SG139 which also has open collector outputs can be used to monitor several additional output voltages. In the application shown in Figure 14, the SG1543 is used to provide both over and under-voltage protection on a main positive supply. The additional comparators within the SG139 can be used to monitor either positive or negative supply voltages depending upon whether one uses the 2.50V signal or ground as the reference potential. The output collectors of each comparator are tied together to the remote activation terminal such that the operation of any single comparator in either the SG1543 or the SG139 will activate the SCR trigger shutdown circuit. Note that grounding the remote activation terminal also provides an output on the over-voltage indicating circuit; therefore, this output on pin 4 can be used as a master power supply-condition indicator which will provide a low signal if any output voltage that is being monitored is outside its allowable tolerance.

SENSING MULTIPLE SUPPLY VOLTAGES

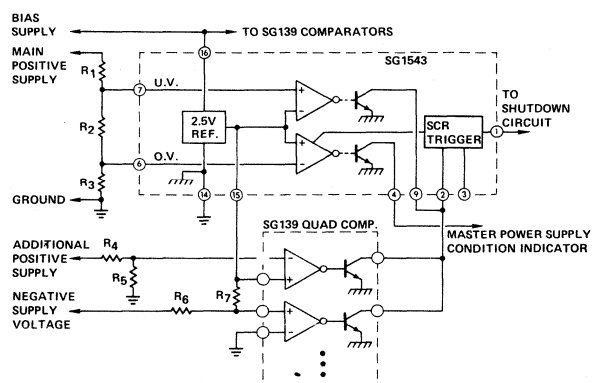

Figure 14. The addition of a simple quad comparator provides multiple voltage sensing for either positive or negative levels.

Under-Voltage Sensing

In addition to normal low-output voltage monitoring, the under-voltage sensing circuit has considerable possibilities in monitoring the input voltage to a power supply system. One quick illustration is given in Figure 15 where this circuit is used to measure the input DC voltage to an SG723 regulator and keep the output completely off whenever the input is lower than the minimum required for satisfactory operation of the SG723. It should be obvious that this same protective feature could be applied easily to a switch-mode regulator where it could be even more important in keeping the switching transistors off until the oscillator stabilizes.

UNDER VOLTAGE SHUTDOWN

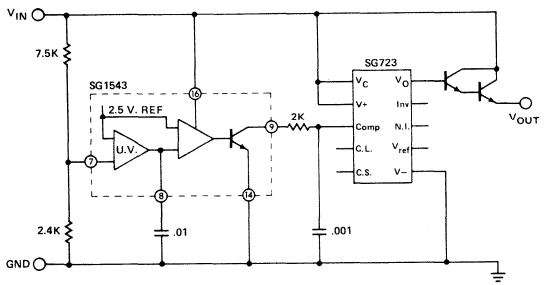

Figure 15. In addition to output monitoring, the under-voltage circuit can be used to inhibit the output if the input voltage is too low for satisfactory performance.

SG1543 INPUT LINE MONITOR

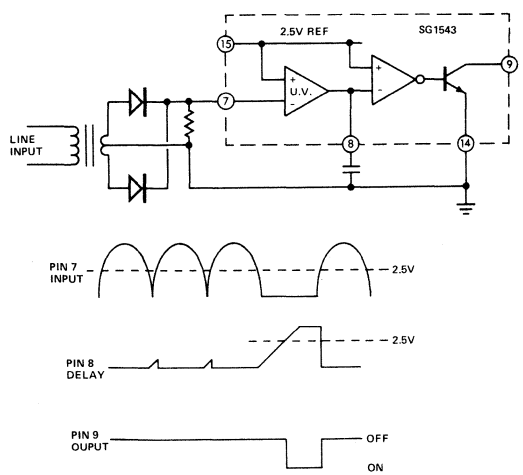

Figure 16. The under-voltage sensing circuit can also be used to monitor the AC input voltage and provide a power failure signal before the power supply output voltage begins to fall.

Another way of using the under-voltage circuit is to monitor the AC input voltage to a power supply system. As shown in Figure 16, an isolation transformer and rectifier are used to provide a rectified AC signal to the input of the under-voltage comparator. The signal is compared with the 2.50V reference, activating the first stage of the comparator with each transition toward zero. With proper selection of the delay capacitor, no output is provided unless some number of input pulses are missing at which time the first comparator allows the charging of the capacitor to 2.50 volts which activates the output circuit. In this way, the under-voltage circuit can be used to monitor the input voltage and provide an immediate indication when it fails, even for as few as one or two cycles. This will provide an early warning indication that the power supply output voltage is going to drop while taking advantage of the holdup capability provided by normal electrolytic capacitor storage within the power supply system.

Like other parts of the SG1543, the under-voltage circuit is not limited to its primary function. Figure 17 demonstrates its use as an over-temperature indicator by using the well-defined temperature coefficent of a darlington transistor's base-to-emitter voltage as a sensor. Divider R1-R2 establishes a fixed threshold which is equal to the 2N2723's VBE at the desired temperature limit. Below that limit, the transistor is off and RC back-biases the input to the U.V. sensor. Although many different transistors could be used for this application, the small case of the 2N2723 makes good thermal coupling relatively easy.

OVER-TEMPERATURE INDICATION

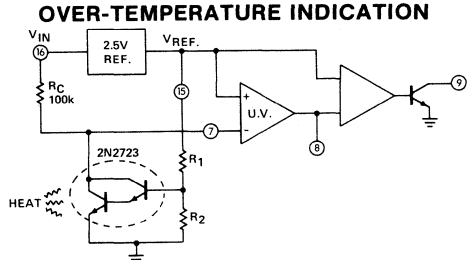

Figure 17. Another use of the under-voltage circuit is to provide an over-temperature indication using the −4mV/° C VBE temperature coefficient of the 2N2723 as a sensor.

By providing all of these diagnostic and protective features within one integrated circuit, a new class of control device has been generated to provide overall performance monitoring and control of sophisticated power supply systems. Thus, the SG1543 further enhances the inventory of building block components available to the power supply system designer providing new options in implementing increased performance at lower cost.

POWER SWITCH DRIVERS: NEW IC INTERFACE BUILDING BLOCKS FOR SWITCHED-MODE CONVERTERS

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Abstract

This paper describes the characteristics and performance of two new integrated circuit products designed to interface between the control circuitry for switch mode converters and their high power output stages. The first device develops the high level turn-on and turn-off commands directly from the outputs of a low power P.W.M. control circuit while the second is designed as a floating switch to control a high current switching transistor directly from the secondary of a drive transformer.

INTRODUCTION

Recent years have seen significant developments by component suppliers which have resulted in the ready availability of many high performance power transistors and sophisticated control integrated circuits for switching power supply design. There existed a gap, however, between the control circuit and the power switching transistors where a considerable amount of circuitry was required to adequately condition and amplify the control signal in such a way as to provide the proper turn-on and turn-off commands to the power switch. This gap has now been filled with two new integrated power switch drivers, the SG1627 Dual Output Driver and the SG1629 High Current Floating Switch Driver.

6

SG1627 DUAL OUTPUT DRIVER

The SG1627 was designed to directly interface between low level control circuitry and the high current handling devices required in switching power supplies. As shown in Figure 1, this is a dual circuit containing both channels that are required for a push-pull system. It accepts the P.W.M. signals from a control circuit such as the SG1524 and provides the conditioning necessary to develop both turn-on and turn-off commands at currents up to 500mA. Its outputs can be used to directly control an external power transistor or to interface with driver transformers for additional power amplification. Another feature of this circuit is the optional ability to provide a constant drive current.

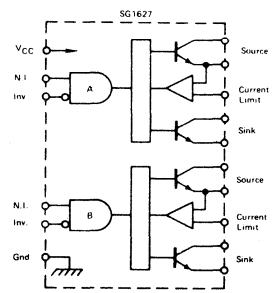


FIGURE 1 – THE SG1627 DUAL OUTPUT DRIVER IS PACKAGED IN A 16-PIN CERDIP D.I.L. PACKAGE.

CIRCUIT DESCRIPTION

Figure 2 shows the schematic for one-half of an SG1627 dual output driver. It must be remembered that there are two identical circuits in each 16 pin dual-in-line package. The inputs to this circuit are switch closures to ground with both inverting and non-inverting logic configurations available. The input threshold level of both logic inputs is 2V, and the logic is

powered by an internal voltage regulator so that input characteristics are unaffected by power supply voltage which can range from 5 to 30 volts.

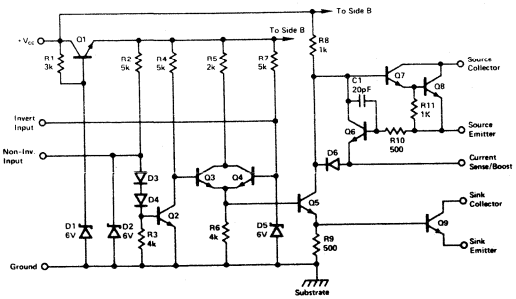


FIGURE 2 – SCHEMATIC DIAGRAM FOR ONE-HALF OF THE SG1627

The output sections of the SG1627 contain both source and sink transistors, each capable of 500mA, 30V operation. In addition, the source transistor has the capability of constant current operation by using an external sense resistor between the source emitter and the current sense terminals. The source transistor is in a darlington configuration which can easily deliver currents to 500mA under all operating conditions but at the cost, however, of a higher saturation voltage. The sink transistor is designed for very low saturation voltage: approximately 0.5 volts at 500mA. It does, however, need greater base drive to meet those high currents. This can be provided either by raising the supply voltage above 5V, or by adding a boost drive current through D6. The saturation characteristics of both source and sink are shown in Figures 3 and 4.

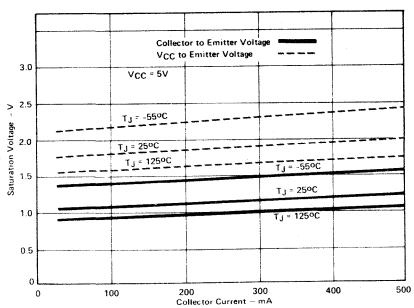


FIGURE 3 – SATURATION CHARACTERISTICS OF THE SG1627 SOURCE TRANSISTOR

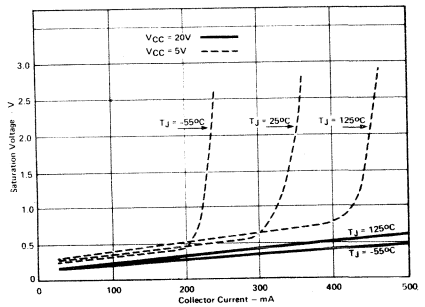


FIGURE 4 – SATURATION CHARACTERISTICS OF THE SG1627 SINK TRANSISTOR

THE TOTEM-POLE OUTPUT CONFIGURATION

One of the simplest uses of the SG1627 is illustrated in Figure 5 where the output is configured to provide a constant 300mA turn-on command to an external switching transistor together with a high peak turn-off current. Note that the logic on the SG1627 is being driven directly from the 5V reference terminal of an SG1524 P.W.M. control I.C. The logic inputs are directly connected to the open collector output transistors of the SG1524 with no additional interfacing components. The output current of the SG1627 comes from the input voltage, which in this case is approximately 10V, but the use of R2 provides a constant source drive regardless of input voltage variations.

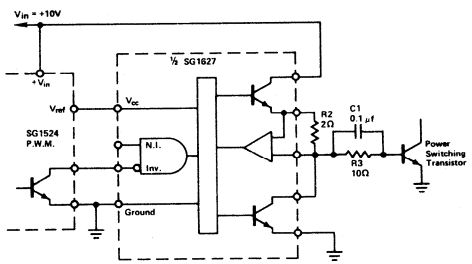


FIGURE 5 – IN A 300mA OUTPUT "TOTEM POLE" CONFIGURATION, THE SG1627 INTERFACES DIRECTLY WITH THE SG1524 REGULATING P.W.M. CONTROL CIRCUIT.

Resistor R3 is used to build up a voltage drop across capacitor C1. At turn-off, the energy stored in C1 provides both a negative voltage to the base of the power switching transistor and the boost drive current necessary to saturate the sink transistor during peak discharge currents of approximately 500mA. With this magnitude of reverse base current (Ib2), transistor turn-off is greatly accelerated.

There are two considerations to remember in this configuration. The first is that the maximum output voltage will be less than the value of Vcc because the source transistor operates as an

emitter follower. With Vcc = 5 volts in this case, the peak output voltage is approximately 3 volts. The other consideration is power dissipation in the source transistor when using it in the constant current mode since it will absorb any excess voltage after current limiting.

The performance of this application is illustrated in Figure 6 which shows the base current into the external switching transistor. One can see both the constant drive current of about 300mA and the rapid, peak negative turn-off current in excess of 500mA. Note that the delays through the SG1627 are less than 50 nanoseconds making a very fast responding circuit.

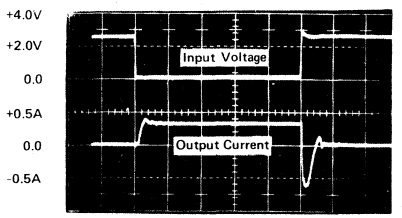


FIGURE 6 – OUTPUT CURRENT TRANSFER FUNCTION

An alternate configuration shown in Figure 7 pictures the SG1627 with a higher value of supply voltage. This offers at least two advantages; first of all, it allows the output voltage swing to rise considerably higher remembering that the source as an emitter follower can rise to approximately 2V below the input supply voltage. The other benefit is in providing greater drive current for the sink transistor allowing 500mA saturation without the need for additional boost current. Because of the large supply voltage across the source transistor, power dissipation can be a problem. This probably means a reduced source current if current limiting is required, although the use of resistor R1 to absorb some of the voltage drop will reduce the power dissipation within the SG1627.

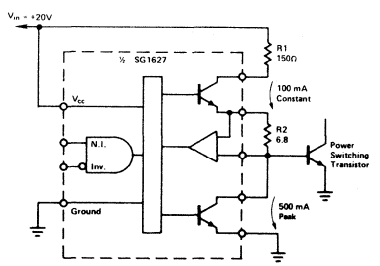


FIGURE 7 – HIGHER INPUT VOLTAGES CAN BE USED TO PROVIDE DRIVE FOR HIGHER SINK-TRANSISTOR CURRENTS

Recognizing the potential for package power limitations, it is important to consider the use of the SG1627 with various types of power boosting circuitry. Maximum flexibility for the use of external current boosting transistors is maintained by the uncommitted availability of both the collector and emitter terminals of both the source and sink transistors. Figure 8, for example, shows the use of an external PNP transistor to boost the source current to 1 amp. The use of the PNP transistor in this configuration still allows current sensing to be used for constant current operation. If constant current operation is not required, an NPN emitter follower booster could also be used. The use of a single boost transistor as shown in Figure 8 makes a powerful drive circuit as one can now drive one amp of turn-on current into a switching power transistor and still have 500mA of turn-off current through the sink transistor.

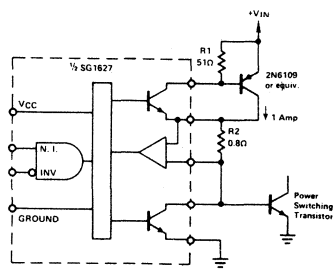


FIGURE 8 – INCREASED SOURCE CURRENT WITH THE USE OF AN EXTERNAL BOOST TRANSISTOR

DUAL PHASE OUTPUTS

The SG1627 does not need to be committed to totem pole operation. The source and sink transistors can be separated and used independently for dual opposite-phased outputs. Figure 9 shows the operation with both source and sink transistor emitters grounded and each used as a common emitter amplifier driving an external load resistor. Figure 9 also shows the use of an external resistor R1 to provide additional drive current boost to the sink transistor. This will allow the sink transistor to provide full 500mA operation with only a 5 volt supply. The response characteristics of this type of configuration are shown in Figure 10, which pictures the response of both source and sink with 24 ohm load resistors to inputs at both the inverting and the non-inverting logic inputs. Note again the minimum delay of both outputs; less than 100 nanoseconds from input to output on both source and sink.

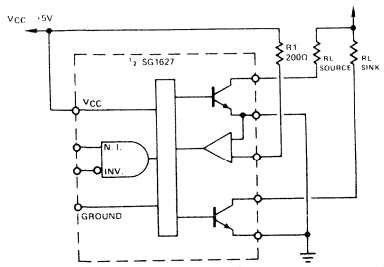


FIGURE 9 – SEPARATE DUAL-PHASE OUTPUTS WITH ADDITIONAL DRIVE CURRENT FOR 500mA SINK TRANSISTOR OPERATION

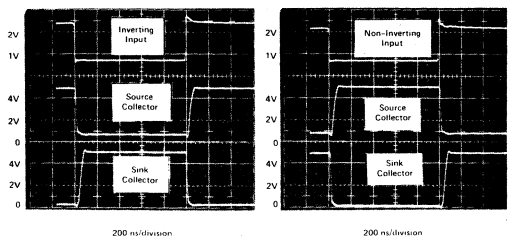


FIGURE 10 – SOURCE AND SINK RESPONSE CHARACTERISTICS

This use of the source and sink as separate outputs provides significant benefit for driving a transformer, as illustrated in Figure 11. In this example, the primary winding of the transformer is driven by the source transistor with its emitter grounded. Constant current operation is shown with the inclusion of the sense resistor, R2, but voltage switching could as easily be accomplished by merely shorting together the sense terminals. To provide greater efficiency in the magnetic design, a reset winding is added and shown being driven by the sink transistor. This ensures that the magnetic flux is reset to zero between each pulse. Of course, the sink transistor opens up every time the source transistor drives the primary winding.

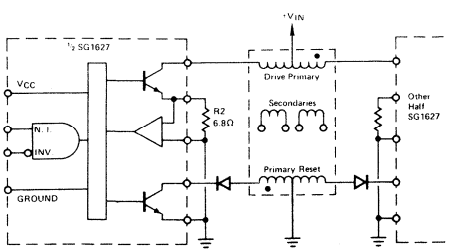


FIGURE 11 – DRIVING AN OUTPUT TRANSFORMER WITH THE SG1627

An additional illustration of the versatility of the SG1627 is shown in Figure 12, where the non-inverting logic input is used to provide a positive guarantee that both sides of a push-pull inverter cannot be on at the same time. This circuit is shown using the inverting input as the primary drive path, which will force the source transistor to be on when the control circuit transistor is conducting. The non-inverting input is then diode-coupled to the opposite side of the inverter and senses saturation of the external power switch. If the collector of the opposite transistor is low, holding the non-inverting input low, then regardless of what happens at the inverting input terminal, the output source on that side cannot be turned on. The sink will remain on, holding the output low until a rising collector voltage on the opposite side removes the non-inverting input at which time the command signal will then come through the SG1627 and turn on the correct side. This circuit is particularly useful as a protection against cross-conduction of the output transistors during transient conditions at power-on or overload.

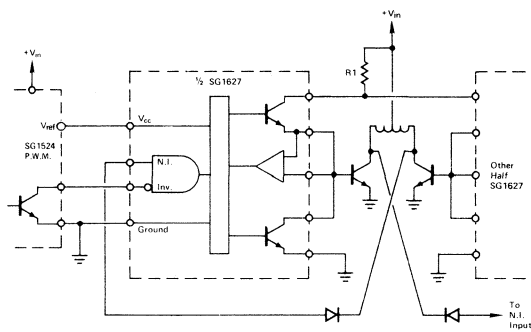


FIGURE 12 – SIMULTANEOUS CONDUCTION OF THE TWO OUTPUT TRANSISTORS IS PREVENTED BY GATING WITH THE NON-INVERTING INPUTS.

The above examples have been chosen to illustrate the versatility and performance of this new device designed to interface between a low level pulse width modulating control circuit and the high power switching transistors used in all modern-day switching power supply designs.

THE SG1629 HIGH CURRENT FLOATING SWITCH DRIVER

A second interface circuit to be discussed in this paper is the SG1629 illustrated in Figure 13. This device has been designed to provide an interface between a drive transformer secondary winding and a high power switching transistor, and again provide the proper signal conditioning to adequately deliver both turn-on and turn-off current into the base of that switching transistor. More importantly, its design is such that it requires no external power connection but develops all the power for

both turn-on and turn-off from the drive transformer and an external storage capacitor. With this capability, the SG1629 can be used in floating operation for bridge inverters at voltages in excess of 300V with respect to ground. This circuit also contains the capability for constant current drive operation with a similar type of current sensing circuit and an external current sensing resistor.

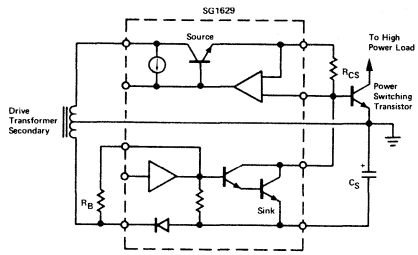


FIGURE 13 – THE SG1629 HIGH-CURRENT, FLOATING SWITCH DRIVER

CIRCUIT OPERATION

The SG1629 functions with a center-tapped drive transformer secondary winding such that when a turn-on command is present and current is flowing in the upper half of the secondary winding through the source transistor and into the base of the power switching transistor, a current is also flowing in the lower portion of the transformer secondary through the high current rectifier to charge the external capacitor C_S to a negative voltage. When the drive command terminates, this negative voltage is used to turn on the sink transistor which then pulls a negative Ib2 current from the base of the switching power transistor down to the negative voltage on the capacitor providing again a high peak turn-off current to speed the response and minimize the power losses in the switching transistor. For maximum versatility, this circuit also contains several gating options.

In Figure 14, the schematic of the SG1629 shows two power darlington transistor structures, each capable of handling an excess of 2 amps of current: Q3/Q4 as the source, and Q6/Q7 forming the sink. Transistor Q5 provides current sensing with feedback to provide constant current operation. The source transistor is turned on by conduction of drive current through resistor R2. The drive current for the source transistor is gated on and off through the action of Q1 which senses the input voltage and provides a turn-off of the source transistor between each drive current pulse.

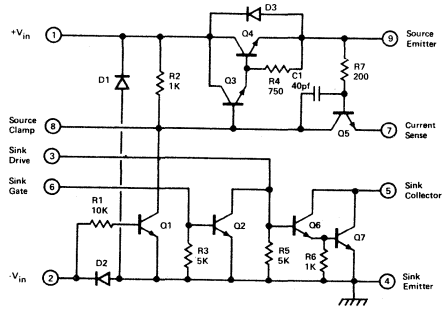


FIGURE 14 – THE SCHEMATIC OF THE SG1629. TRANSISTORS Q4 AND Q7 ARE DESIGNED FOR TWO-AMP OPERATION.

The darlington sink transistor has its input brought out as a separate sink drive terminal which gives the user several driving options. In addition, the sink driving current can be gated by the use of Q2, which has its own input terminal. The diodes D1 and D2 are high current rectifiers which provide the charging current for the external capacitor attached to the sink emitter terminal. The action of transistor Q1 to gate the source transistor insures that there is negligible discharge current (less than 10mA) from the external capacitor during the off periods of the circuit. This allows the capacitor to be charged with very narrow drive pulses separated by relatively long off periods.

The SG1629 is packaged in both a multi-pin TO-66 power package and an 8-pin minidip. Having no sensitive, low-current circuitry, this device can be operated with a maximum junction temperature of 175°C which, coupled with a low Θ5C thermal resistance of 5°C/W, gives the TO-66 package a 3 Watt capability in free air and 10 Watts or more with some heat sinking. Because of the versatility of this device, it was felt that there may be applications for lower power requirements and thus the SG1629 will also be available in an 8-pin ceramic minidip package which, of course, has a power dissipation of only 800mW. With one pin less in the 8-pin minidip package, the sink gating function is sacrificed.

SG1629 APPLICATIONS

The use of the SG1629 can best be demonstrated in an application as shown in Figure 15 where two SG1629's are used to provide the drive signals for the power transistors in a 5 amp one-half bridge switching supply. The drive transformer is shown with 10 volt drive signals on the primary winding which, with a 2:1 transformer turns ratio, provides a 5V peak signal on each half of the secondary. When the drive command is present on one secondary, it is translated into a constant current through the source transistor by the use of the sense resistor,

Rcs, which, in this case, provides a constant 700mA into the base of the external NPN transistor. At the same time, the 20 microfarad external capacitor is being charged with a current through the rectifier in the SG1629 and the lower half of the secondary winding. While this is occurring, the opposite phase signal is being applied to the lower SG1629 circuit which serves to further enhance the charge on its external capacitor while maintaining the power switch in the off state.

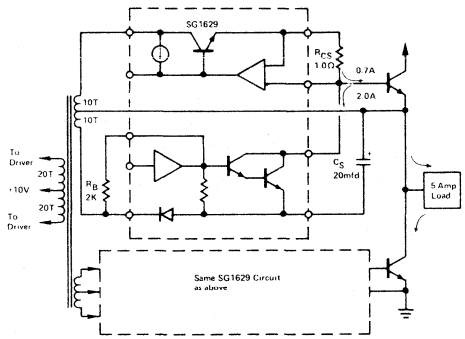
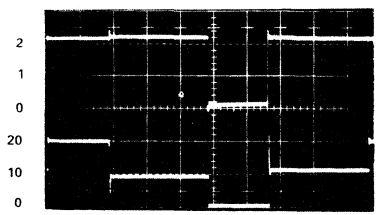


FIGURE 15 – USE OF THE SG1629 IN A 5-AMP, HALF-BRIDGE CONVERTER

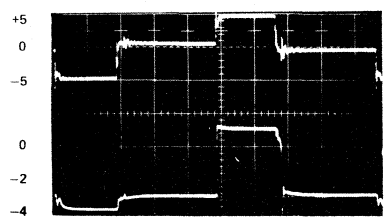
When the drive command terminates, the voltage at both ends of the secondary winding goes to zero. Since there is approximately -4V at the emitter of the sink transistor while its base is being driven through the external drive resistor, RB, to zero volts, the sink transistor then immediately turns on and pulls a high current Ib2 pulse out of the external transistor and through the capacitor. This current, of course, only flows as long as it is available from the stored charge within the base of the external transistor as the source has been gated off. After that charge is depleted, the sink transistor remains on insuring a negative reverse voltage at the base of the switch transistor.

The performance of the SG1629 can be illustrated by the waveform photographs in Figures 16 through 18. In Figure 16, the command signal from one channel of the control circuitry and the waveform of the drive transformer primary voltage are shown. The voltage on the secondary winding, referenced to the centertap and the power transistor emitter, is pictured in Figure 17. Also shown in this photograph is the input voltage at the base of the external NPN transistor. Note that at the very first portion of this waveform, when the opposite side is on, there is an additional negative charge supplied to the capacitor so that we have a maximum reverse base-to-emitter voltage of close to -4V. During the off time, the action of the sink transistor maintains a negative voltage bias of approximately -3V on the base of the power transistor. When the drive command is given to turn on, the base voltage goes positive to the 0.7 or so volts necessary to turn it on and at turn-off, goes negative again. The important action is shown in Figure 18 which pictures the actual base current of the power transistor with a scale of one amp per division. Both the constant turn-on Ib1 of about ¾ amp and the peak Ib2 of close to -2 amps can be seen along with the collector voltage waveform with a 5 amp resistive load. Remembering that the time base of all these waveform photographs is 5 microseconds per division, one can see approximately one microsecond delay between the turn-off signal at the base and the actual turn-off of the collector of the output transistor. Although this turn-off response is primarily a function of the transistor design, it is safe to say that any power switching transistor should perform faster with this form of base drive.



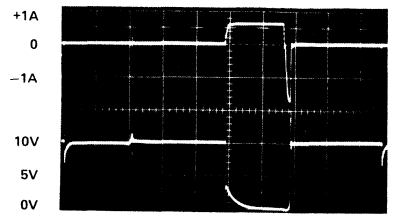
Time Base: 5 μSec/Division
Upper Trace: P.W.M. Control Signal
Lower Trace: Drive Transformer Primary

FIGURE 16 – INPUT CONTROL TO THE DRIVE TRANSFORMER



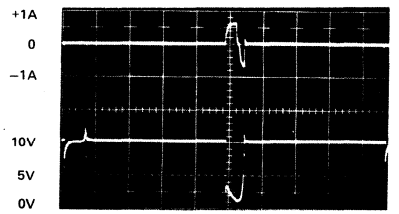
Time Base: 5 μSec/Division
Upper Trace: Drive Transformer Secondary
Lower Trace: Power Transistor Base Voltage

FIGURE 17 – THE BASE VOLTAGE DELIVERED TO THE EXTERNAL POWER SWITCHING TRANSISTOR BY THE SG1629



Time Base: 5 μSec/Division
Upper Trace: Transistor Base Current
Lower Trace: Collector Voltage with $R_L = 2\Omega$

FIGURE 18 – BASE CURRENT AND COLLECTOR VOLTAGE OF THE EXTERNAL SWITCHING TRANSISTOR



Time Base: 5 μSec/Division
Upper Trace: Transistor Base Current
Lower Trace: Collector Voltage with $R_L = 2\Omega$

FIGURE 19 – OPERATION WITH NARROW PULSE WIDTHS

Note that one can also see in the collector waveform a soft knee at turn-on where the power transistor is not saturated instantaneously. This is partially because of the turn-on characteristics of the transistor and partially because of the finite rise time of base current through the driving circuitry. This rise time is primarily a function of the leakage inductance of the drive transformer which opposes a sudden change in current from zero to maximum value. It is an exercise in transformer design to configure the transformer to minimize to the greatest extent possible the leakage inductance. This can be done with a minimum number of turns and a maximum coupling between turns. In the illustration, a ferrite pot core of approximately ¾" in diameter was used to configure the drive transformer. More will be said about turn-on rise time later, but first let's discuss one additional characteristic of concern in the turn-off circuitry: The operation with very narrow pulse command.

Since the charge on the external capacitor is developed during the turn-on command, narrow pulse widths accomplish the transfer of a minimum amount of energy. As the drive command pulse widths get narrower, there is a point where the voltage on the external capacitor begins to fall off. With the circuit components as shown earlier, this loss of Ib2 occurs at approximately 2 microsecond pulse widths. Figure 19 shows the base current and collector voltage waveforms at narrow pulse widths where the Ib2 has diminished from 2 amps down to approximately ¾ of an amp. Further reductions in pulse width bring the Ib2 current ultimately to zero. This characteristic is, of course, a function of the time constants in the total circuit and some compromise or optimization can be achieved by appropriate selection of capacitor values and secondary drive voltages.

The above circuit incorporated constant current drive which is an advantage if the load current happens to be relatively constant but in many applications this is not the case. The SG1629 may also be used to provide a base drive proportional to load demand by adding an anti-saturation clamp diode as shown in Figure 20. With the current sense terminals shorted, there are two V_{BE} voltage drops between the clamp and source emitter terminals. Therefore, the clamp diode D1 will hold the collector on voltage to approximately one diode drop above the base. This will keep the switching transistor right at the threshold of saturation, regardless of load current variations.

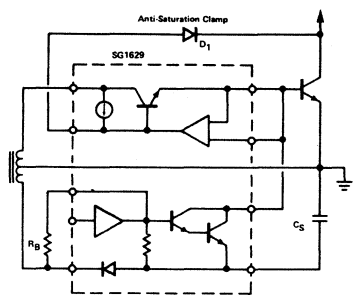


FIGURE 20 – USE OF THE SG1629 IN A LOAD-DEPENDENT DRIVE CONFIGURATION

IMPROVING TURN-ON RESPONSE

In applications where maximizing base current rise time is important and secondary transformer inductance is a significant consideration, the use of the gating functions in the SG1629 can provide significant benefits. Figure 21 shows the addition of an external transistor Q1 to drive the sink transistor's gate circuit. To explain the operation of this circuit, note that the sink transistor's base drive is now being generated with RB connected to the common or center tap of the drive transformer secondary instead of the negative input terminal. This is essentially zero volts and since the emitter of the sink transistor

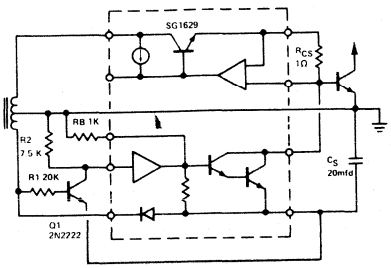


FIGURE 21 – IMPROVING BASE CURRENT TURN-ON RISE TIME

is attached to the capacitor which has a negative voltage on it, the sink transistor would normally be on continuously. Transistor Q1 is selected as a relatively slow non-gold-doped transistor which has a finite storage time. Its action is to turn the sink transistor off during the drive command signals, but to delay that off signal for some increment in time. Note that before the commencement of a drive command, the sink transistor is on by the action of RB. Transistor Q1 is also saturated by its base resistor being connected to the end of the transformer which is also at zero volts prior to the command signal.

When the drive command is initiated, current begins to build up in the secondary circuit and the first flow of current is through the source transistor, through the current limiting resistor, down through the sink transistor which is still conducting, and back to the negative terminal on the transformer secondary. The switching transistor is still back-biased while this occurs. Because the input to transistor Q1 is now at a negative voltage, it turns off, but since it has a finite storage time, that time is used to delay the rise of the input to the sink gate. Additional delay can be added with a small capacitor at the sink gate input terminal. When the input to the sink gate goes high, its output goes low, forcing the sink transistor to turn off. Since the source current is already flowing, turn-off of the sink diverts that current to the base of the output transistor producing an Ib1 rise time of less than 100 nanoseconds.

When the action is reversed at turn-off, there is negligible increase in delay between the turn-off signal and the actual turn-on of the sink transistor. This is because Q1 is the only device with a long storage time and it is turning on so storage is not a factor.

Another method of speeding up the rise time of current into the base is the use of some reactive components to differentiate the drive current signal. A simple approach is a capacitor by-pass around the current sense resistor, Rcs, providing an initial boost in turn-on current.

GETTING IT ALL TOGETHER

The overall simplifications which Silicon General has offered to the design of switch mode power converters can best be illustrated by Figure 22 which shows the total command signal flow from the feedback error information to the output of a high current half-bridge regulating inverter. The SG1524 was designed to provide all of a switching regulator's P.W.M. control signals with the only external components required being the divider resistors to interface with the error amplifier, the overall loop compensation network, and the resistor and capacitor to set the operating frequency. The SG1524 drives the SG1627 directly which, in turn, provides the signal conditioning to develop the drive and reset commands to an interstage drive transformer. The secondary windings of that drive transformer are directly coupled into a pair of SG1629 floating drivers which are then used to command the external 5 amp switching transistors which form the high power output stage of the power supply.

These circuits have all been designed to offer a maximum degree of flexibility while incorporating what would otherwise be a substantial amount of discrete circuitry.

Thus, all these new IC's greatly ease the design and manufacturing problems typically inherent in switching power supplies and, at the same time, provide greater repeatability and reliability at significantly reduced costs.

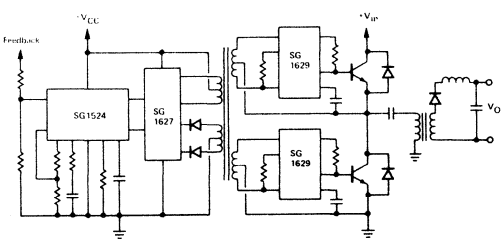


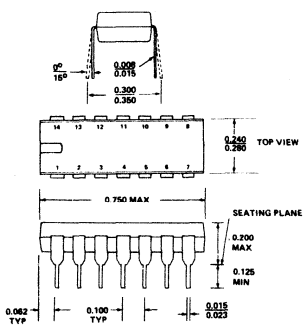
FIGURE 22 – THREE IC TYPES FORM A MAJOR PORTION OF THE CONTROL ELECTRONICS FOR A SWITCH-MODE HALF-BRIDGE CONVERTER.

Package Outlines

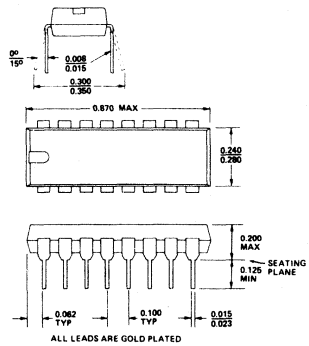
SILICON GENERAL PACKAGE RATINGS

Package Type	Thermal Resistance (°C/W)				Power Dissipation (mW)	Derate above 25°C (mW/°C)
	θ_{JC}		θ_{JA}			
	Typ.	Max.	Typ.	Max.		
K (TO-3)	3.0	5.5	35	45	4300	30
P (TO-220)	3.0	5.0	60	65	2000	16
R (TO-66)	5.0	6.0	40	50	3000	24
T (TO-39)	15	25	120	185	1000	6.7
T (TO-99)	25	40	150	190	680	5.4
T (TO-96)	25	40	130	165	800	6.8
T (TO-100)	25	40	150	190	680	5.4
T (TO-101)	25	40	150	190	680	5.4
J (16-pin)	45	60	80	110	1000	6.7
J (14-pin)	45	60	80	110	1000	6.7
Y (8-pin)	50	60	125	150	800	8
N (16-pin)	50	60	130	150	600	6.0
N (14-pin)	50	60	130	150	600	6.0
M (8-pin)	50	60	160	190	400	4.0
F (10-pin)	40	60	170	190	500	3.3

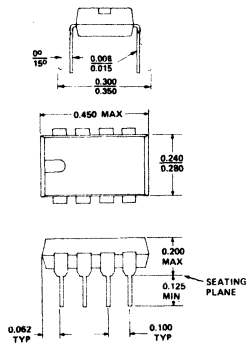
PLASTIC PACKAGES



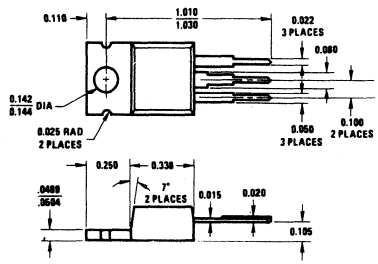
N-PACKAGE
14-PIN PLASTIC



N-PACKAGE
16-PIN PLASTIC

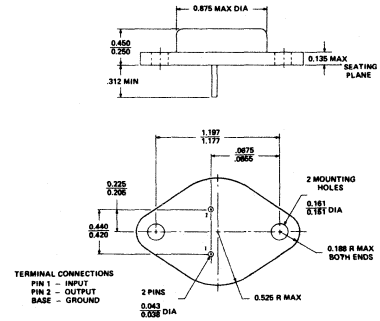


M-PACKAGE
8-PIN MINIDIP

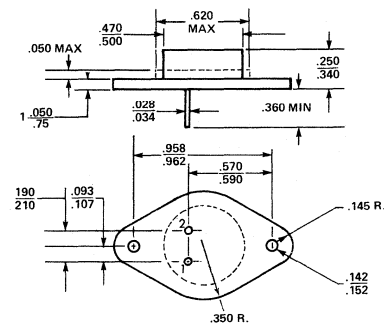


P-PACKAGE
TO-220

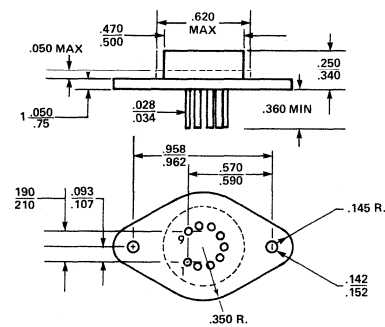
POWER PACKAGES



K-PACKAGE
TO-3

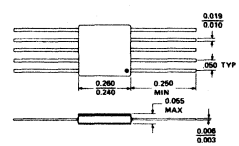


R-PACKAGE
TO-66, 2-PIN



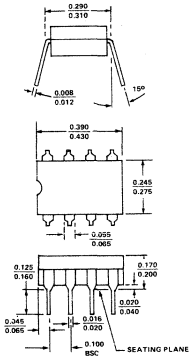
R-PACKAGE
TO-66, 9-PIN

FLATPACK

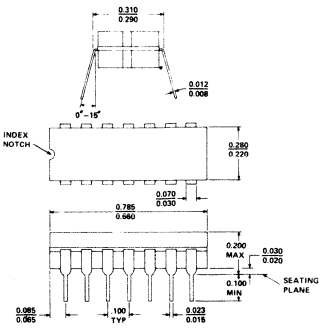


F-PACKAGE
10-PIN FLATPACK

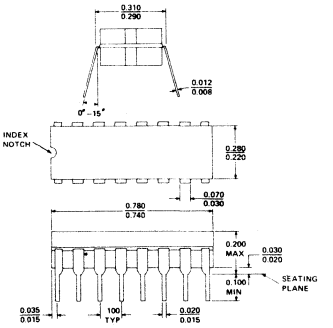
CERAMIC PACKAGES



Y-PACKAGE
8-PIN CERDIP

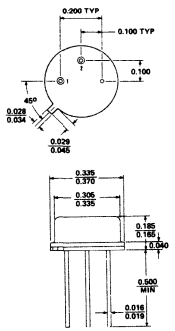


J-PACKAGE
14-PIN CERDIP

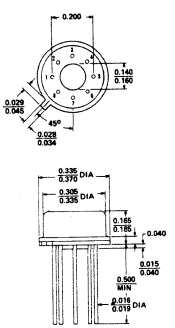


J-PACKAGE
16-PIN CERDIP

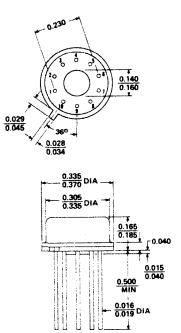
METAL CANS



T-PACKAGE
TO-39



T-PACKAGE
TO-99



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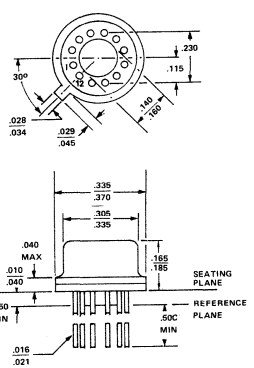

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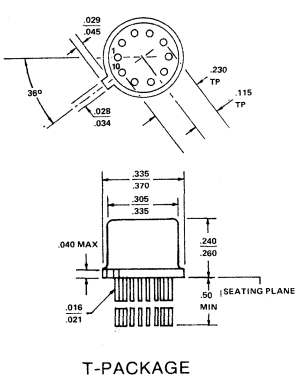
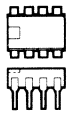
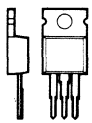
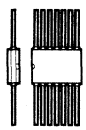
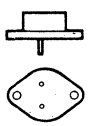
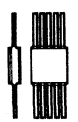
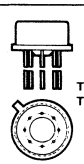
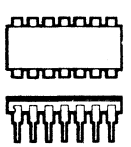
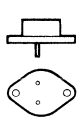


T-PACKAGE
TO—96

INDUSTRY PACKAGE CROSS-REFERENCE

	Silicon General	NSC	Signetics	Fairchild	Motorola	TI	RCA	AMD	Raytheon
 Plastic DIP			V						N
8-Lead	M	N	A	T	P	P	E	PC	DN
									DP
14 and 16-Lead	N		B	P	P	N	E	PC	MP
 TO-220 (Package 26)	P	T	U	U		KC			
 Low Temperature Glass Hermetic Flat Pack	F	W		F	F	W		FM	
 TO-66									
3 Lead	R				R				R
9 Lead	R								TK
 Glass/Metal Flat-Pack	F	F	Q	F	F	F, S	K	F	J, F, Q
 TO-5, TO-39, TO-96, TO-99, TO-100 and TO-101	T	H	T, K, L, DB	H	G	L	S*, V1**	H	T, H
 Low Temperature Ceramic DIP									
8-Lead	Y	J	F	R	L	J	–	–	DC
14 and 16-Lead	J			P					DD
 TO-3 (Steel)	K	K					K		K,
(Aluminum)		KC	DA	K	K	K			LK,

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